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B365

Version : 11

CPU :

Intel CoffeeLake-S

System Chipset :

Intel KabyLake-H Chipset

On Board Chipset :

IMVP8 -- NCP81220+NCP81258 7Phase

Gigabit LAN -- RTL8111HN

HDA Codec -- Realtek ALC623

Super I/O --NCT6686D-L

SPI Flash 128Mb + 64Mb

Main Memory :

2 Channel DDR 4 * 4 (Max 64GB)

Expansion Slot :

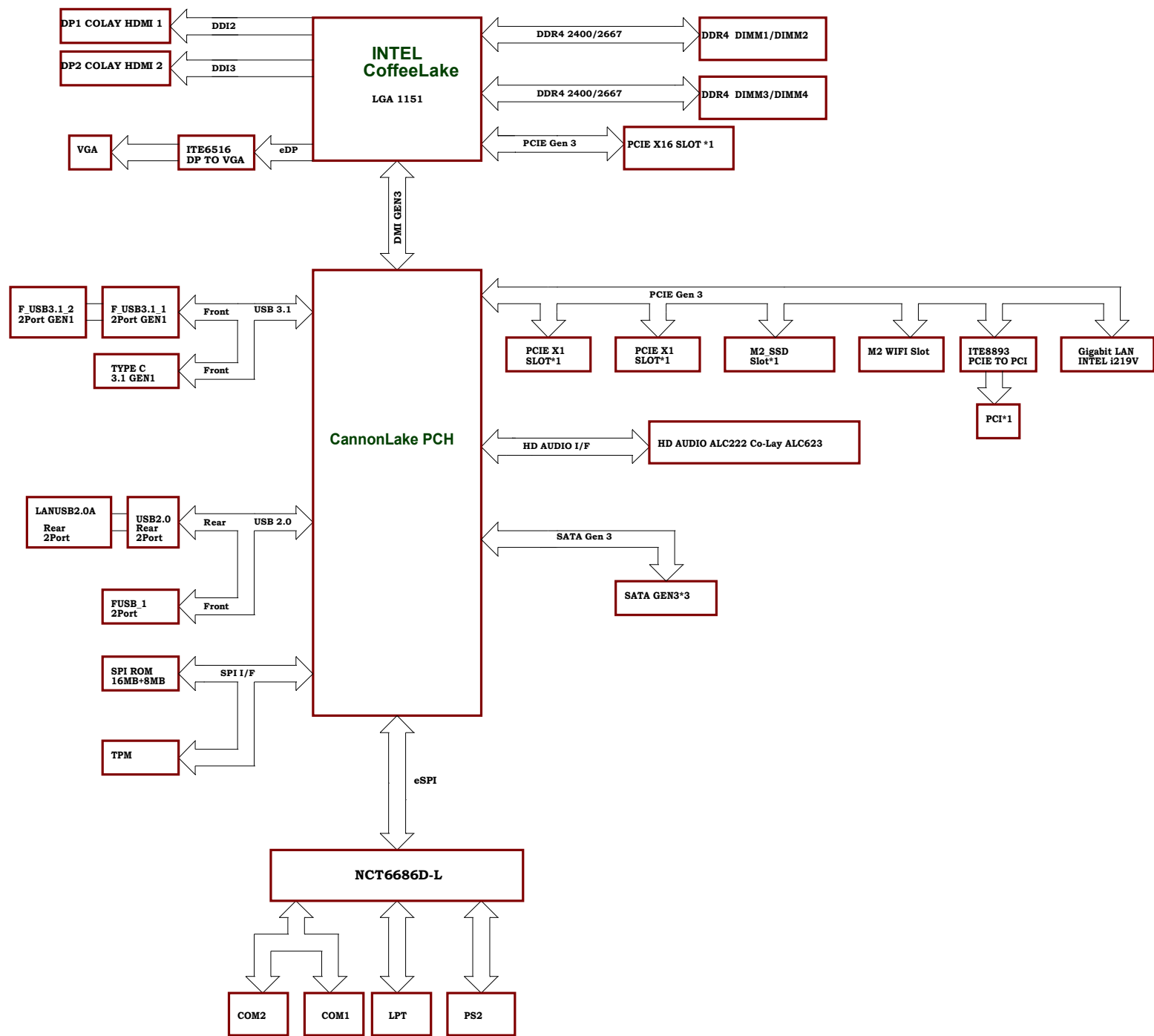
PCI Express x16 Slot * 1

PCI Express x4 Slot * 1

PCI Express x1 Slot * 1

PCI SLOT * 1





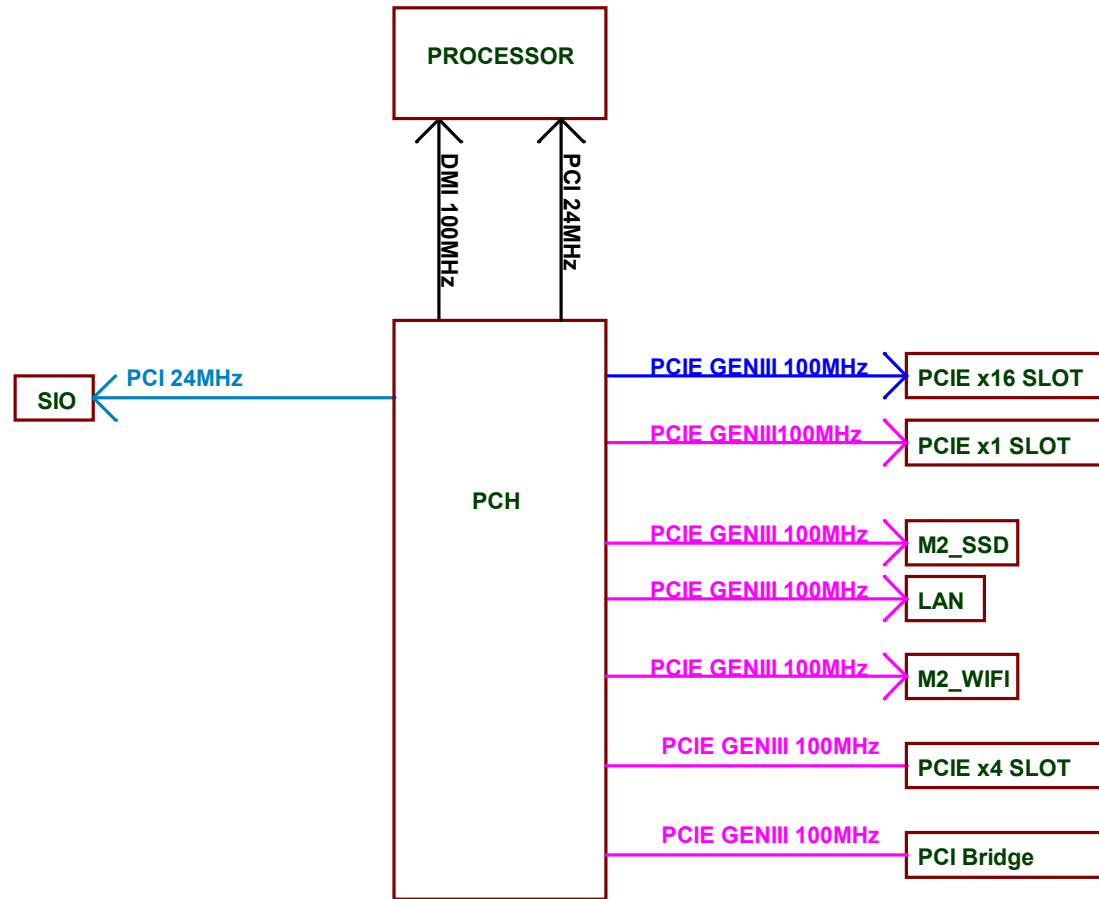
Slot Sequence:

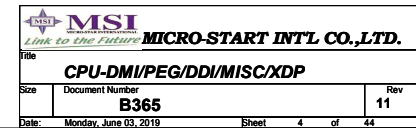
PCIE X16

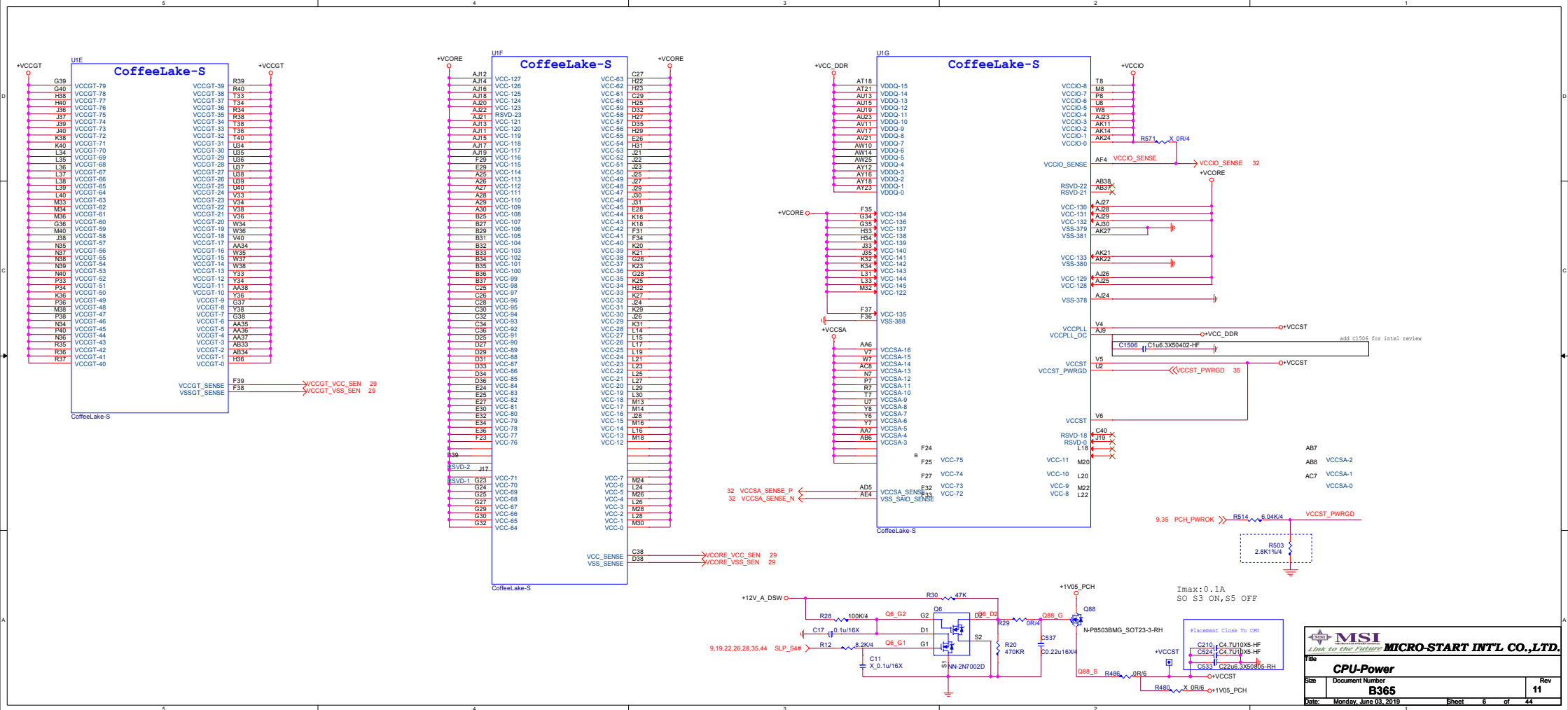
PCIE X1

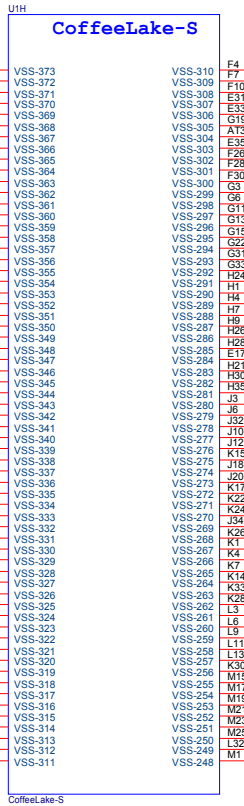
PCIE X16(signal x4)

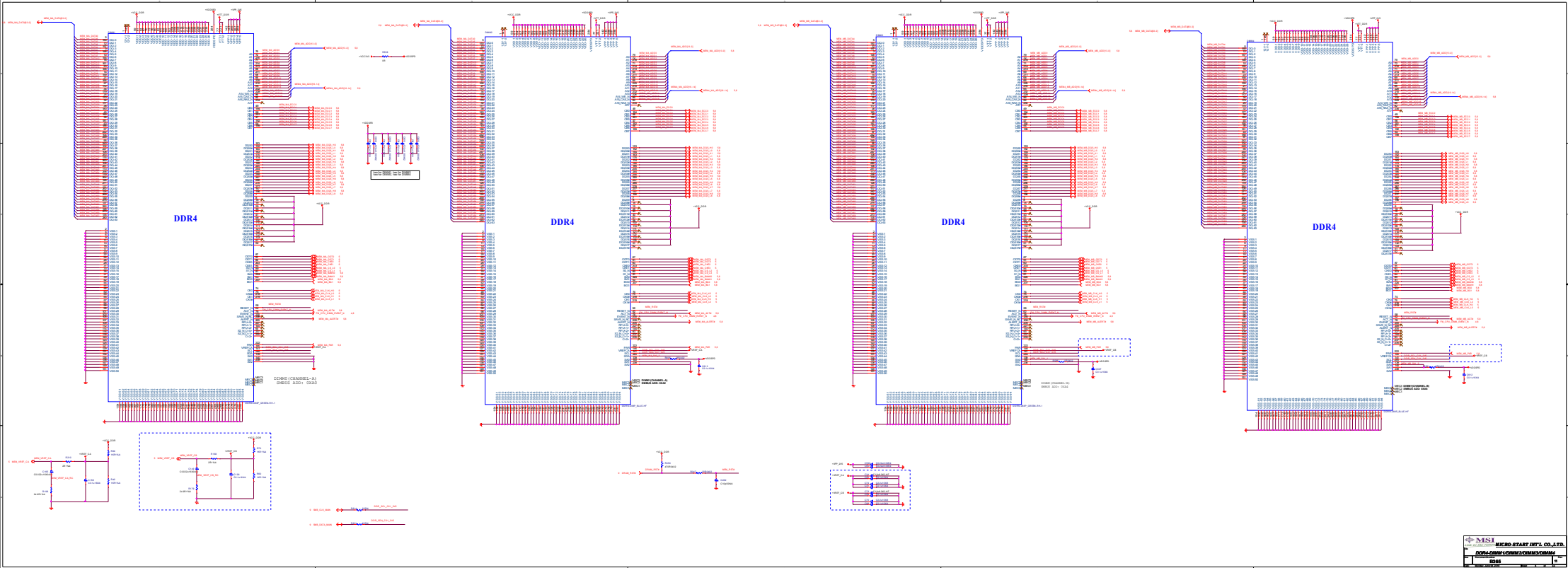
PCI SLOT

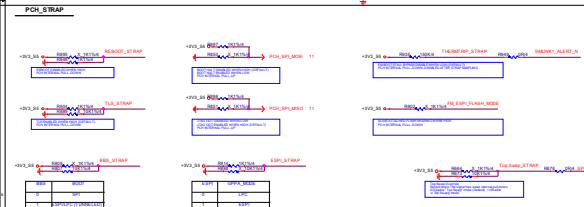
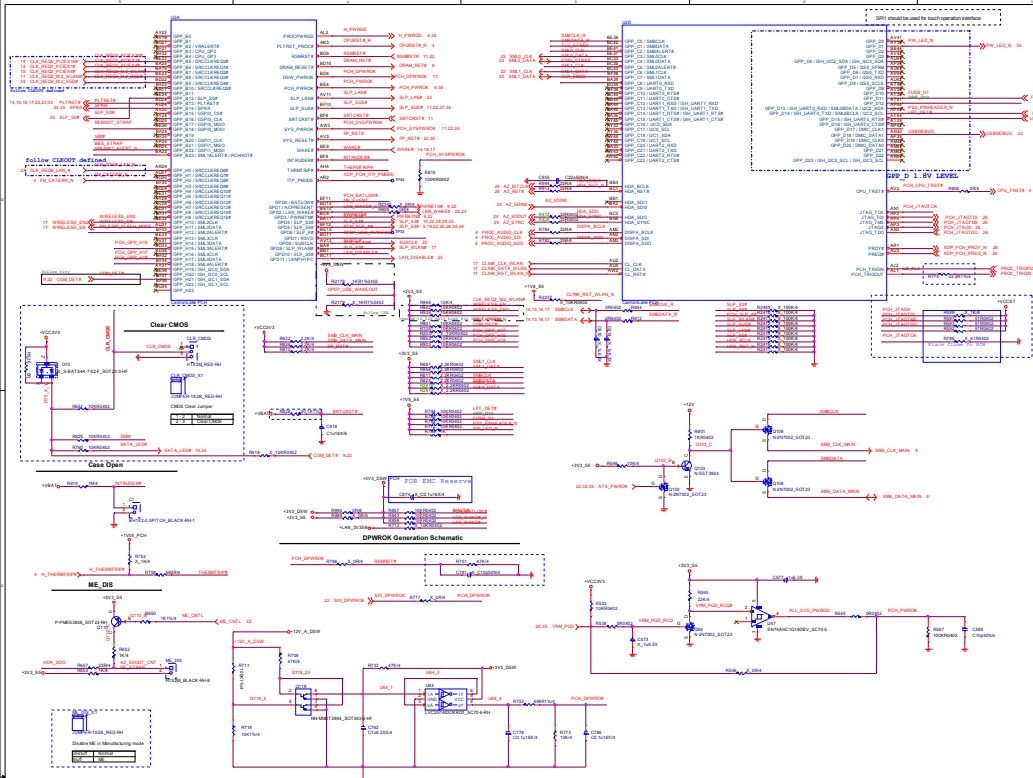


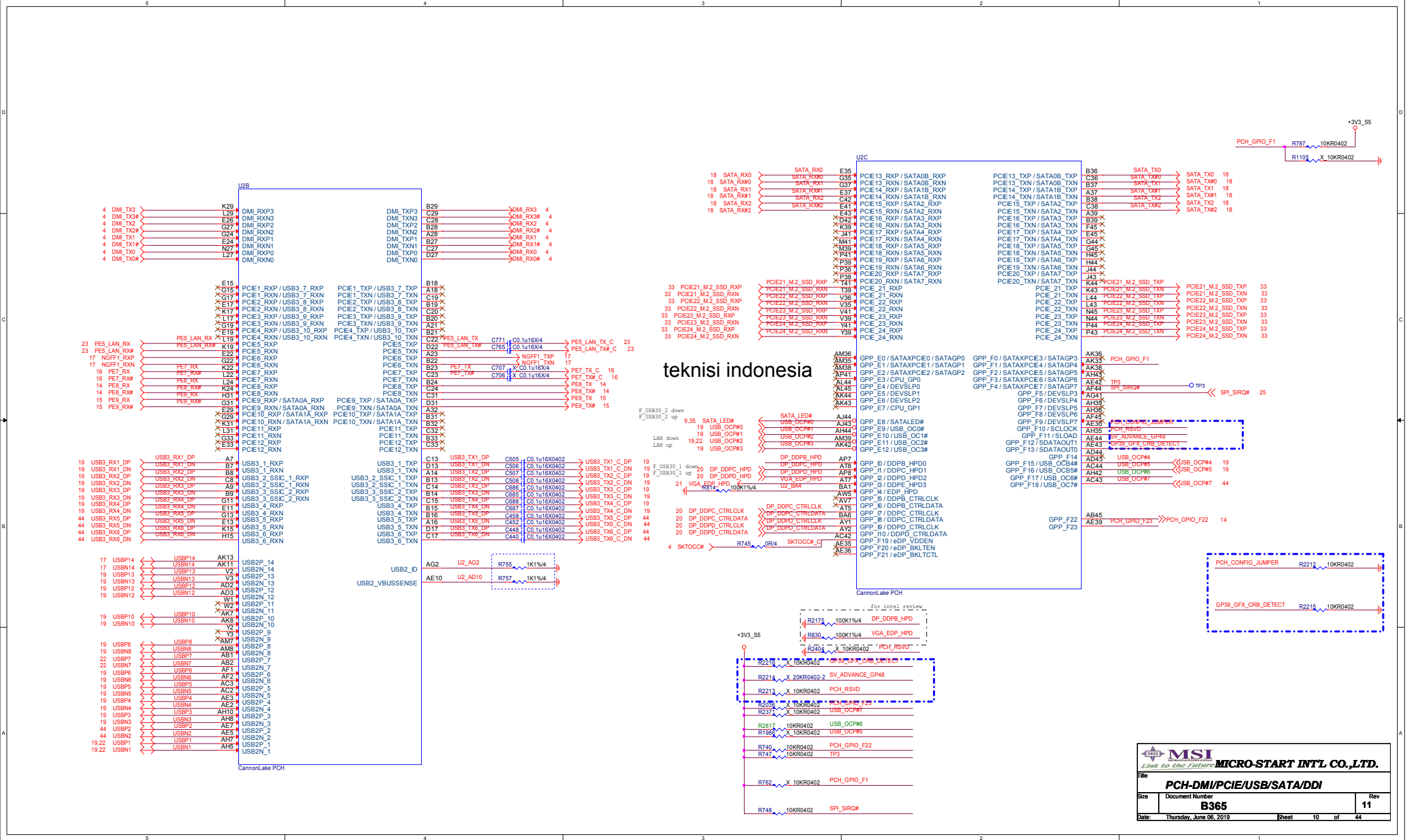




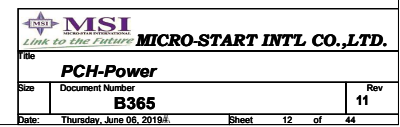


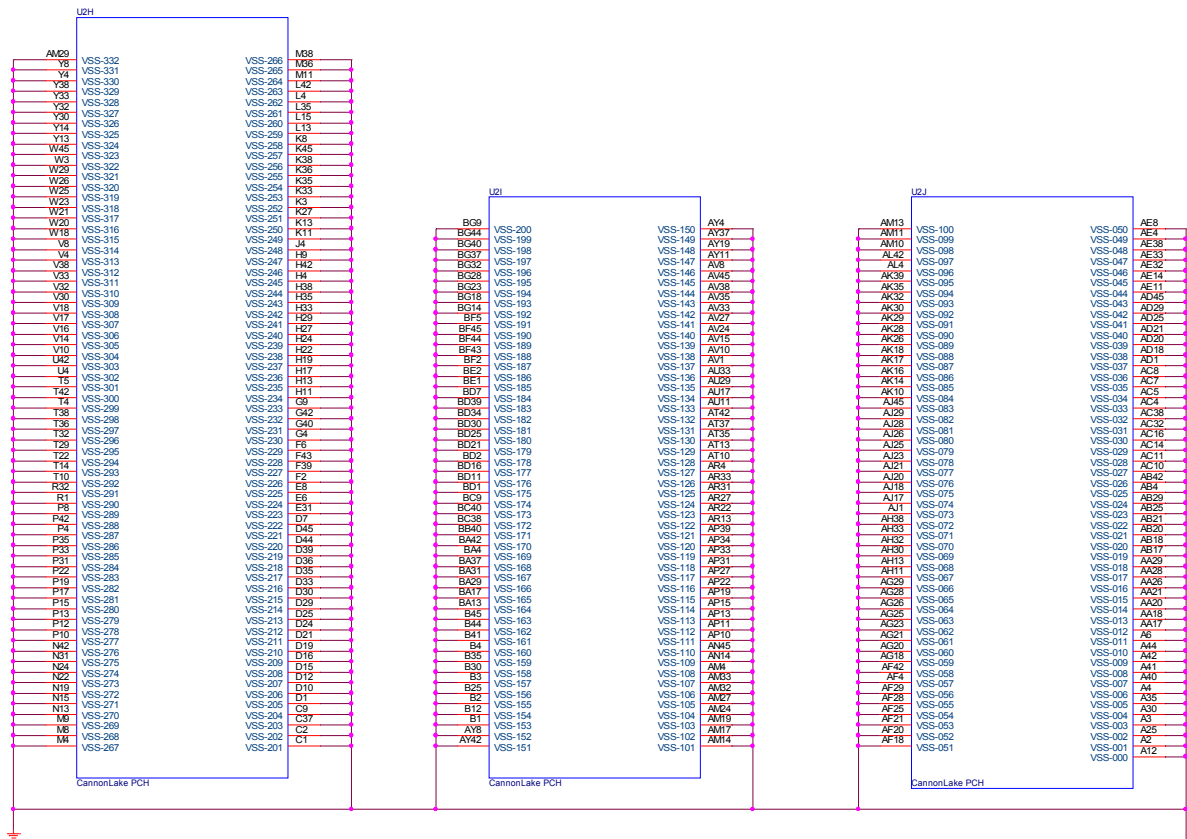




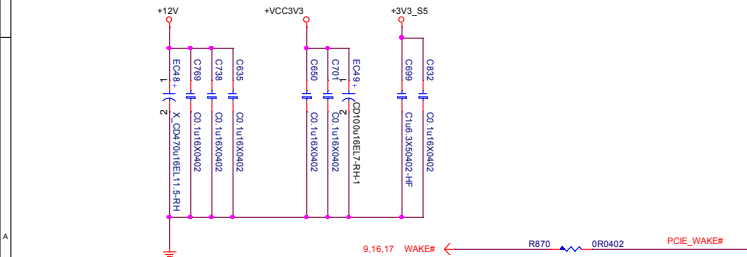


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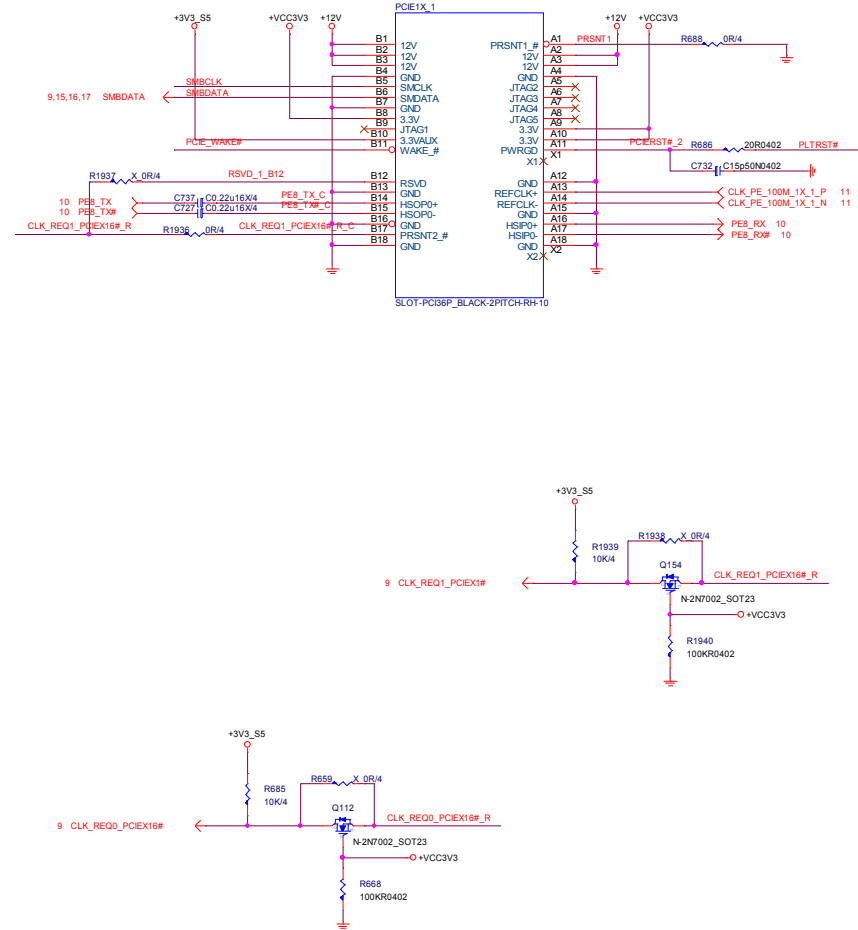




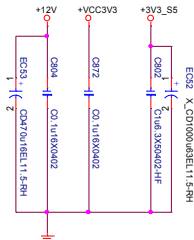
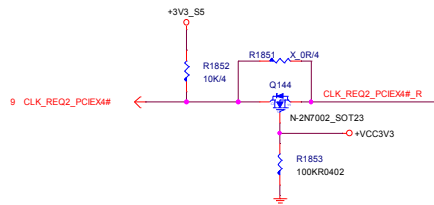
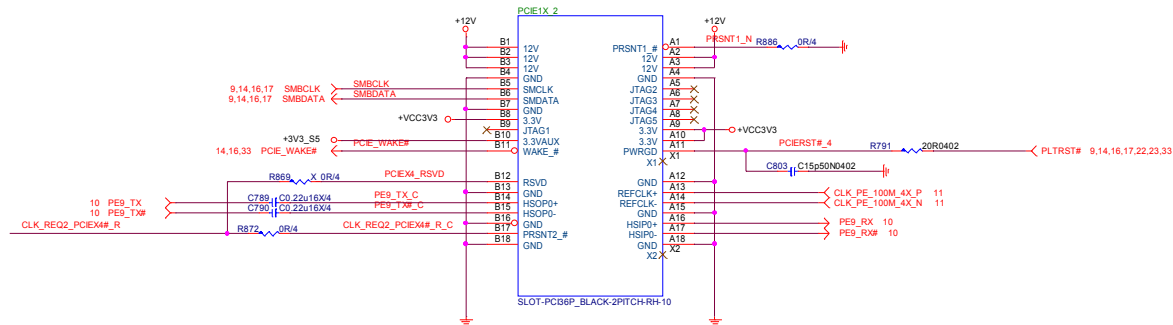
PCIE16X_1

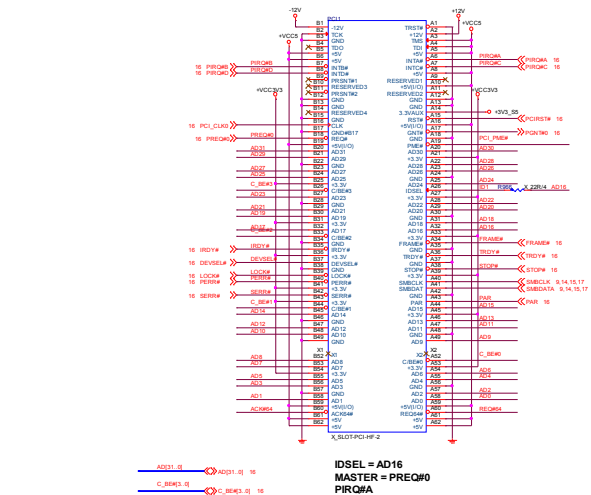
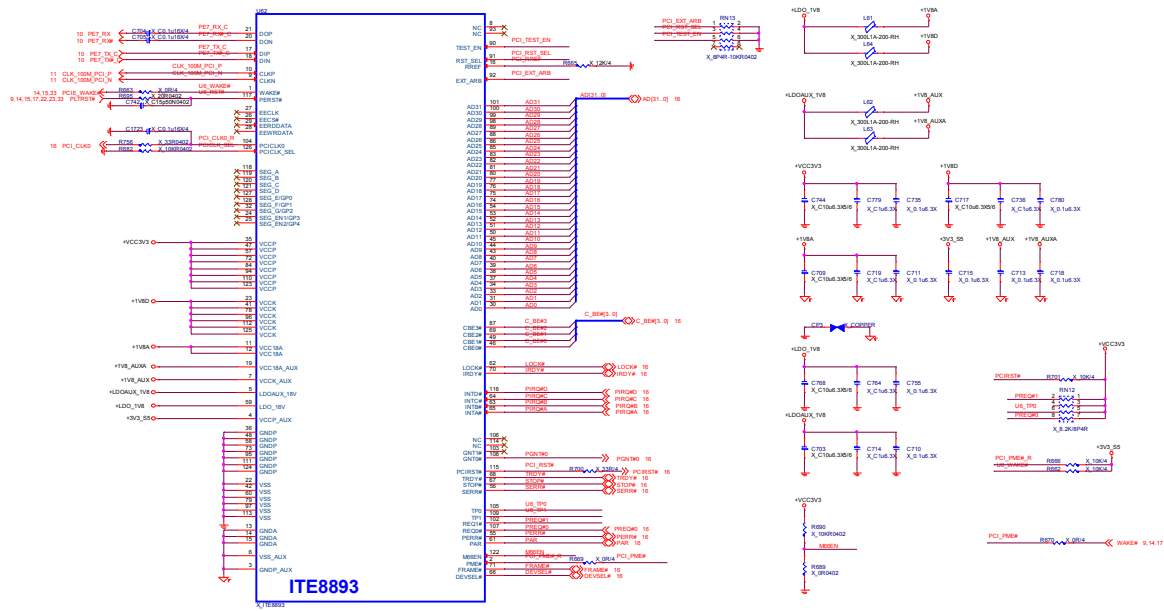


DCIEAY.4

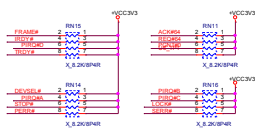


PCIE EXPRESS X1

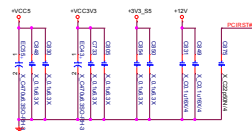


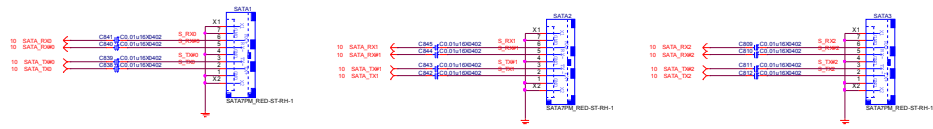


PCI PULL-UP / DOWN RESISTORS

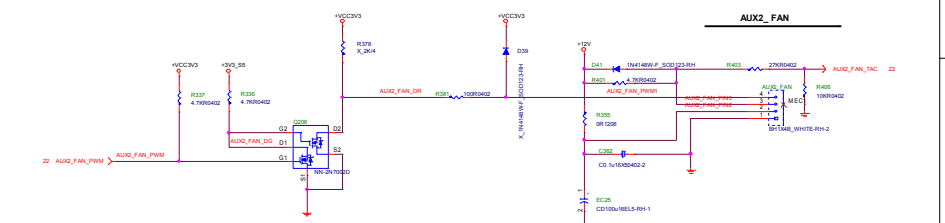
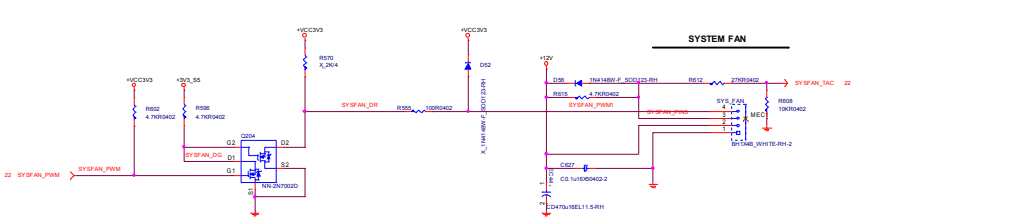
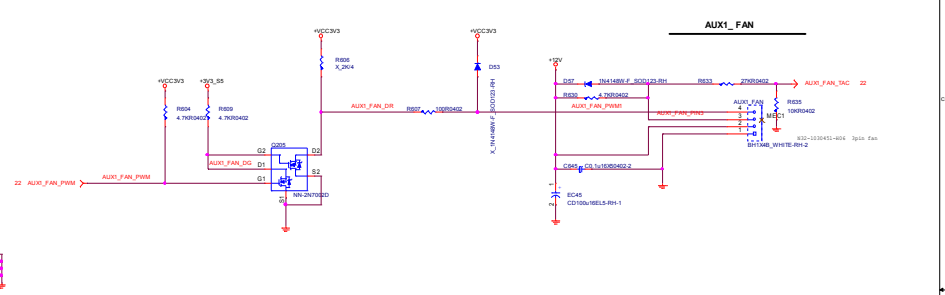
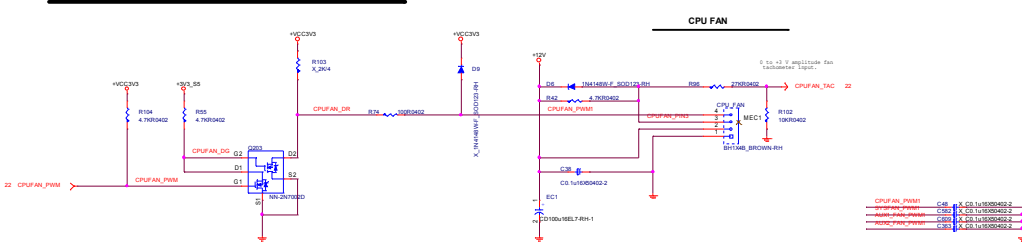


PCI slot		
+3VSB (wake)	-	375mA
+3VSB (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5A
+12V	-	0.5A



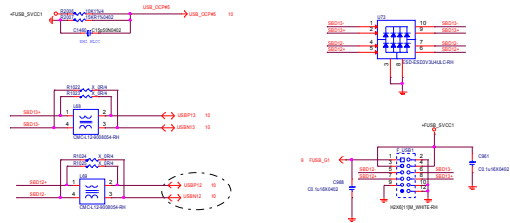


CPU FAN /SYSTEM FAN /POWER FAN

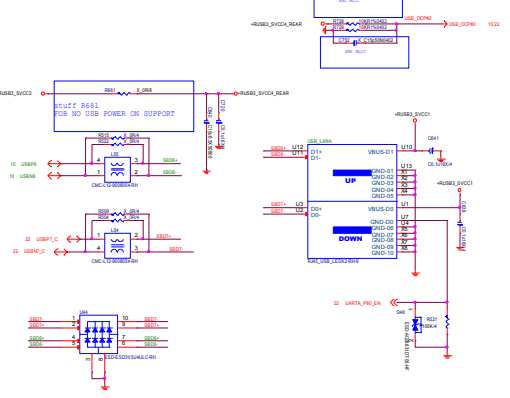


Front Panel USB Connector For USB Port 3 / 4

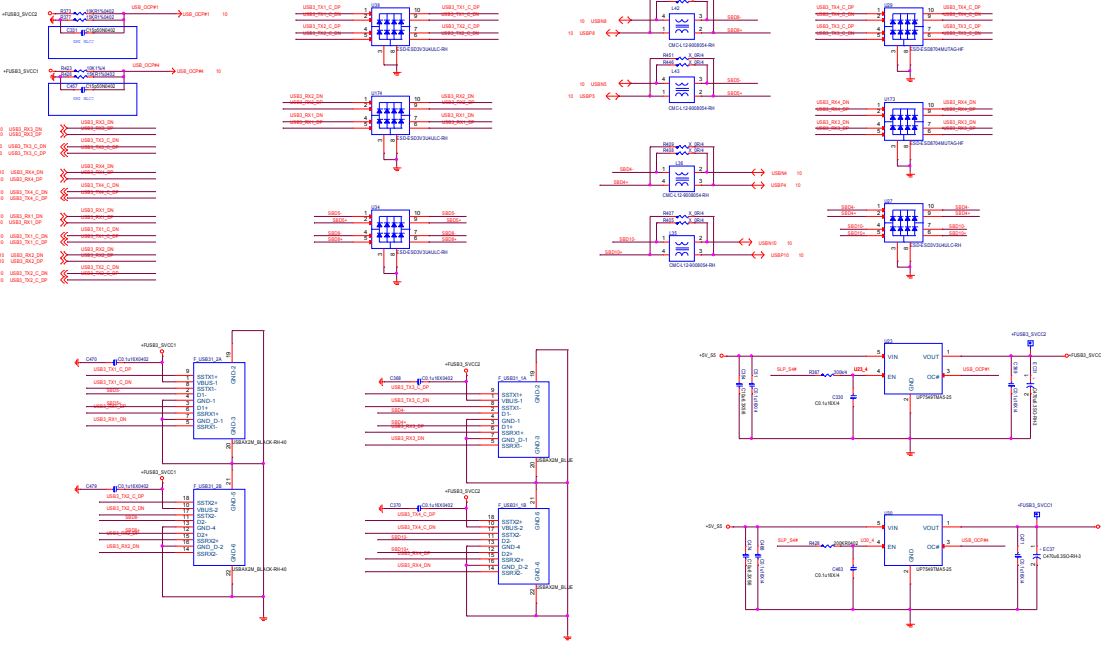
Front Panel USB Connector For USB Port 1/2



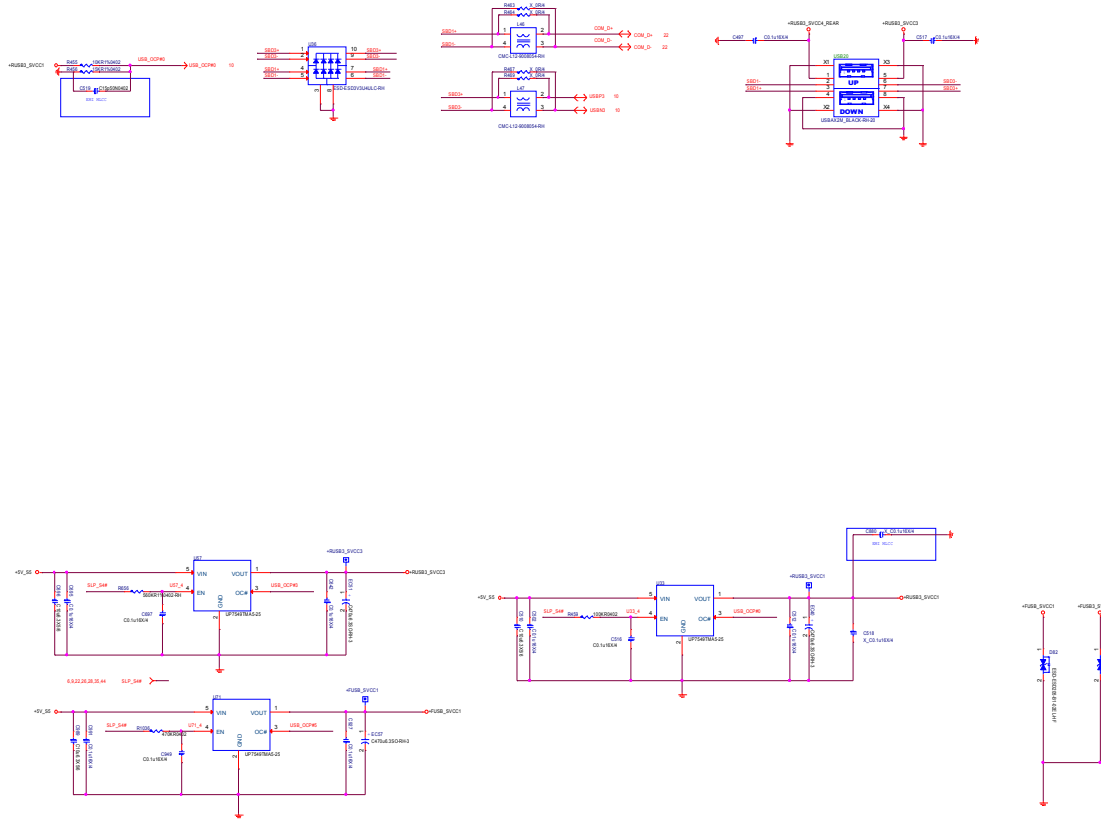
Rear USB Connector For USB Port 9 / 10



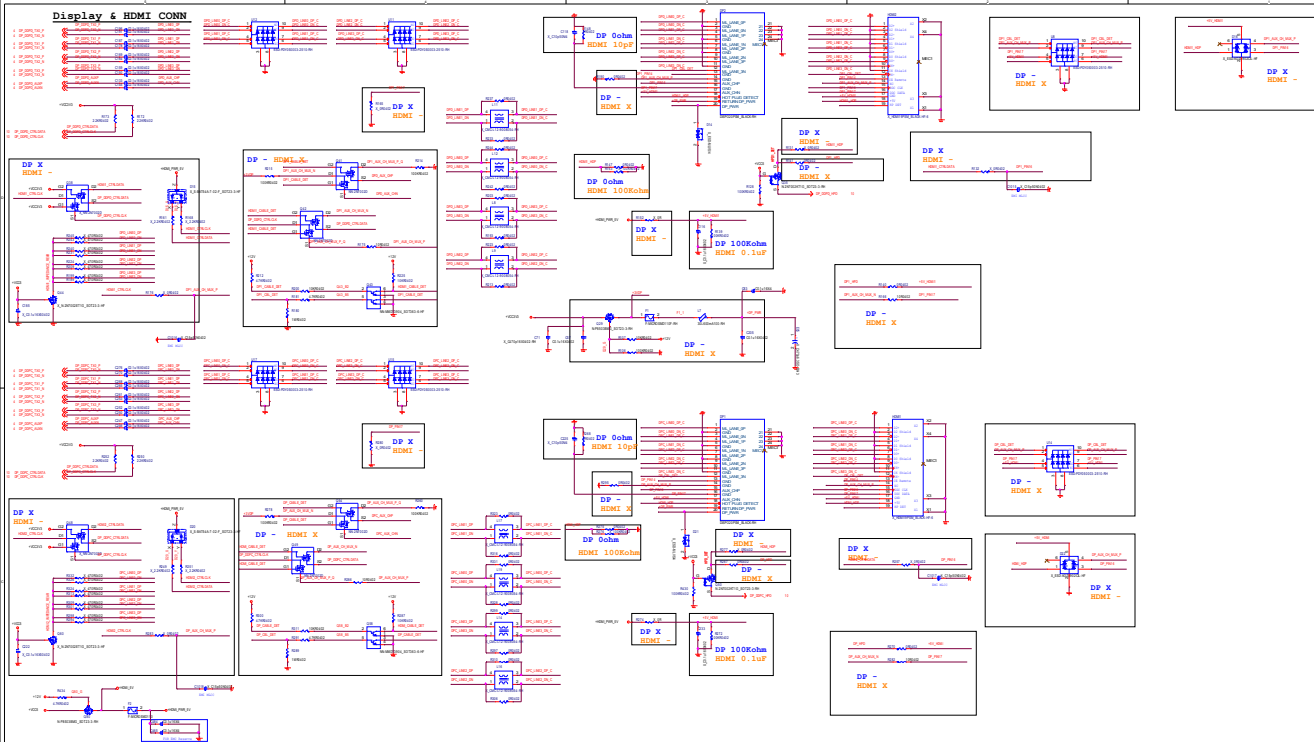
Front IO USB Connector For USB Port 3/4



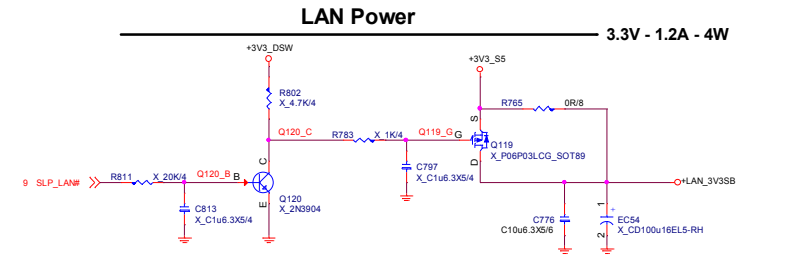
Rear IO USB Connector For USB Port 7/8



The figure consists of four schematic diagrams arranged in a 2x2 grid, each showing a different DP-HDMI interface configuration. The top-left diagram is labeled 'DP to HDMI' and shows a complex circuit with multiple multiplexers and demultiplexers. The top-right diagram is labeled 'DP to HDMI X' and shows a similar but more complex circuit. The bottom-left diagram is labeled 'DP to HDMI' and shows a simpler circuit. The bottom-right diagram is labeled 'DP to HDMI X' and shows a circuit with a different topology. A legend at the bottom right defines the symbols for DP to HDMI, DP to HDMI X, and DP to HDMI. The diagrams illustrate the signal flow and component connections for each interface type.







1.2 definition for LC

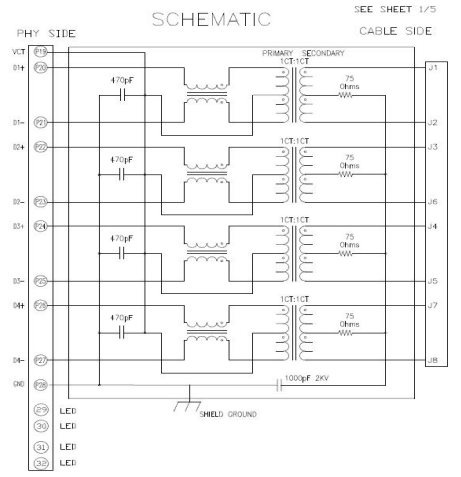
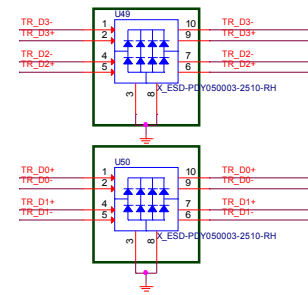
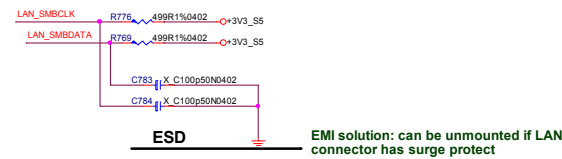
(1) LAN LED Status

(2) Yellow: Domain Wavelength (A) 582.5nm, Luminous Intensity (b) 12.50mcd.

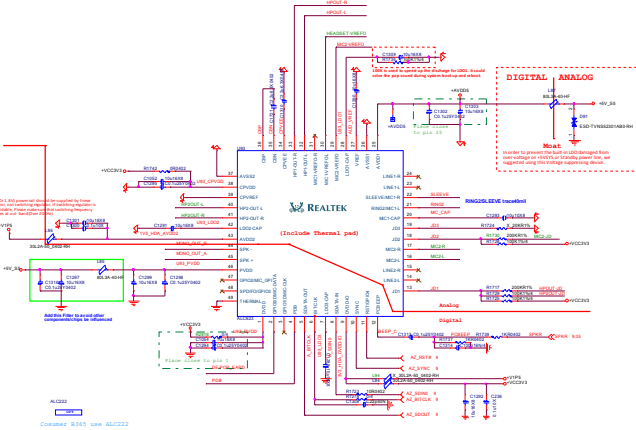
WCOL	status	Yellow:
don't care	No Link	off
off/HiZ WCOL and Host WCOL should be disable (both)	S3/S4/S5	off
on	100M_inactive	
on	100M_active	
on	100M_inactive	
on	100M_active	
on	1G_inactive	
on	1G_active	

always on

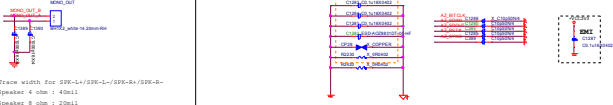
blinking



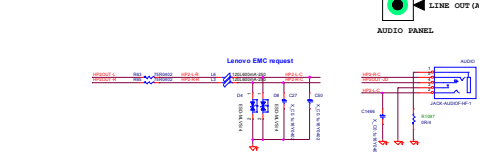
Azalia Codec - ALC222 Co-Lay ALC623



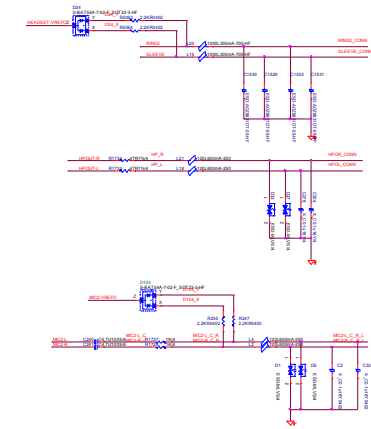
MONO Amplifier



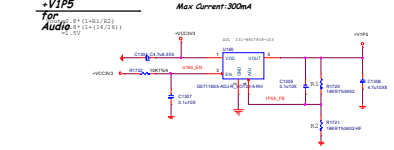
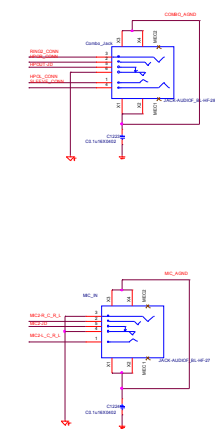
REAR IO



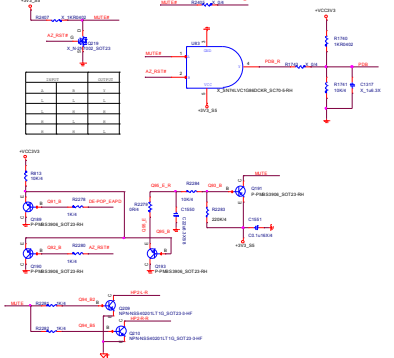
Front AUDIO PANEL



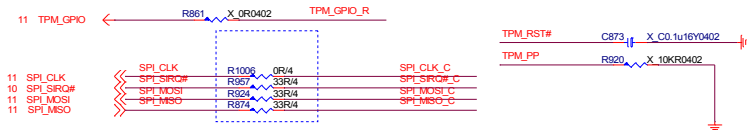
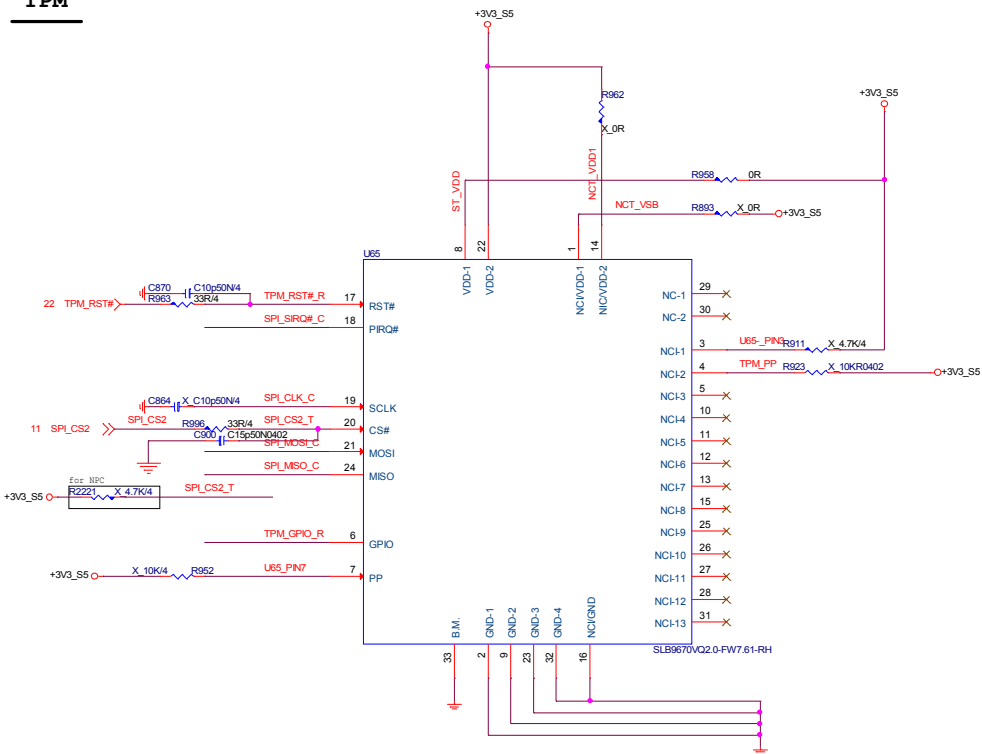
supported iPhone and Nokia headset



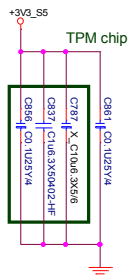
Audio DE-POP

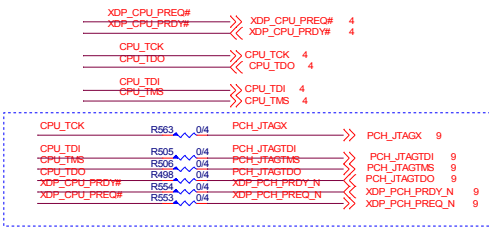


TPM

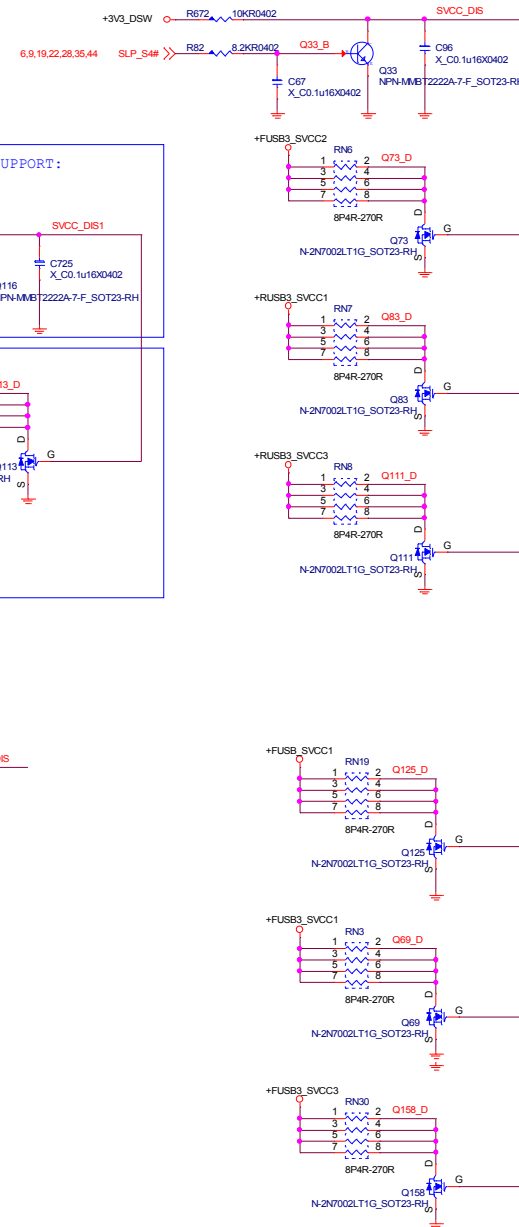
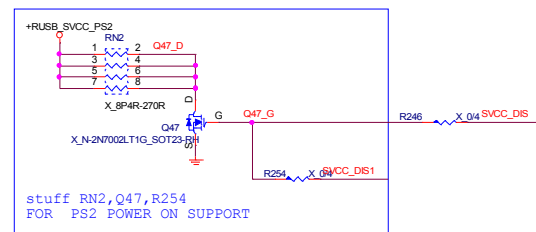
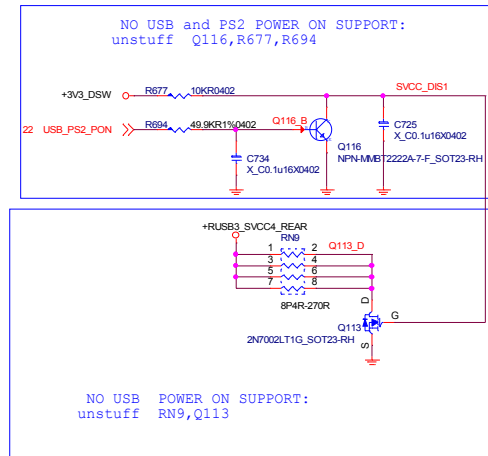


	R893	R911	R923	R920	R952	R958	R962	R861
ST----ST33HTPH2E32AHB4 (SPI)	X	X	X	X	X	X	X	X
NPC---NPCT750 (SPI)	V	X	X	X	X	V	V	X
Infineon SLB 9670VQ2.0 (SPI	X	X	X	X	X	V	X	X





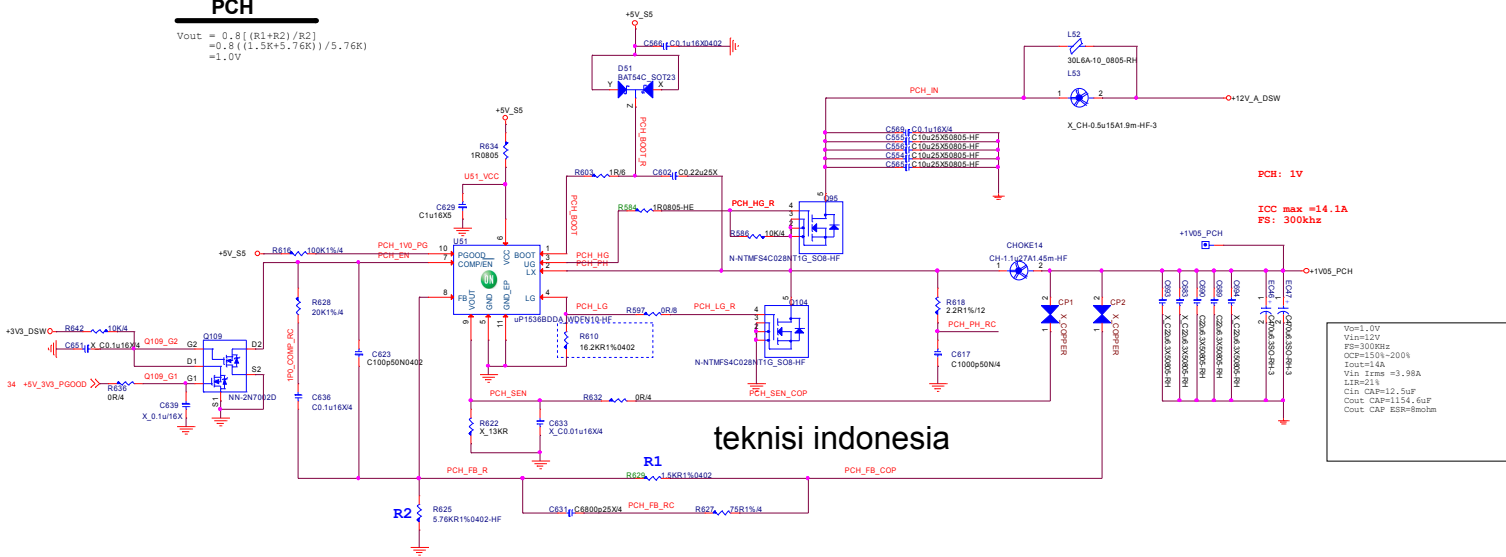
USB power discharge circuit



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PCH

$$V_{out} = 0.8 \left(\frac{R1+R2}{R2} \right) \\ = 0.8 \left(\frac{(1.5K+5.76K)}{5.76K} \right) / 5.76K \\ = 1.0V$$

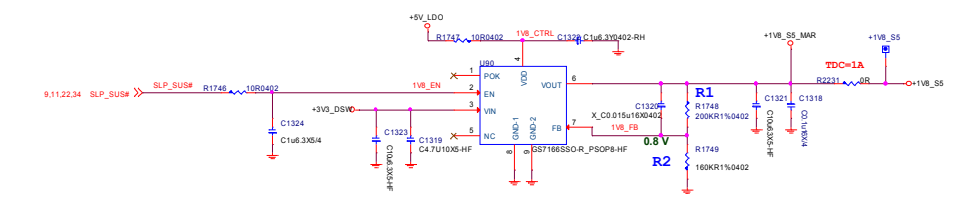


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Vin=1.0V
Vout=1.0V
FS=300kHz
OC=150%~200%
Iout=1.4A
Vin I rms =3.98A
I2PR=21.9
Cin CAP=12.5uF
Cout CAP=1154.6uF
Cout CAP ESR=8mohm

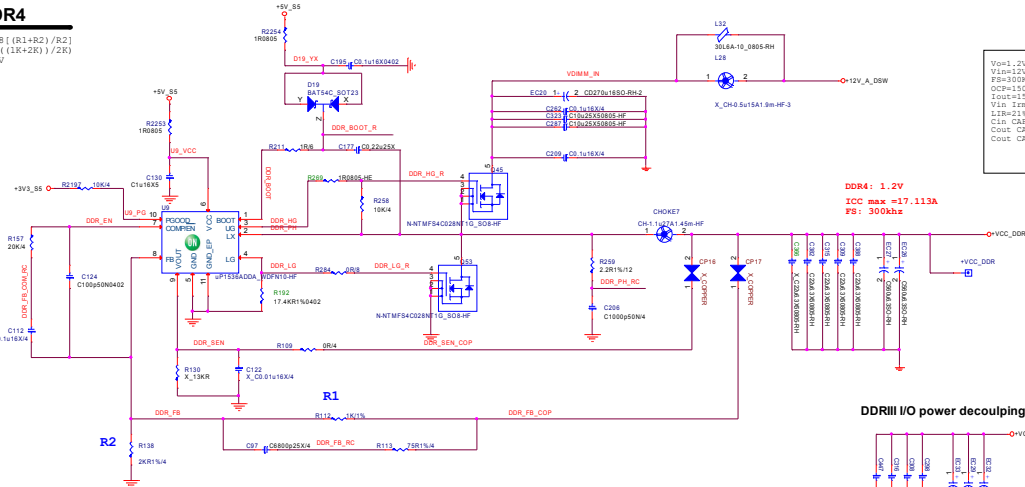
+1V8_S5

$$V_{out} = 0.8 \left(\frac{R1+R2}{R2} \right) \\ = 0.8 \left(\frac{(15K+12K)}{12K} \right) / 12K \\ = 1.8V$$

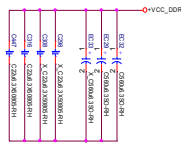


DDR4

$$V_{out} = 0.8 \left(\frac{R1+R2}{R2} \right) \\ = 0.8 \left(\frac{13+28}{28} \right) / 28 \\ = 1.2V$$

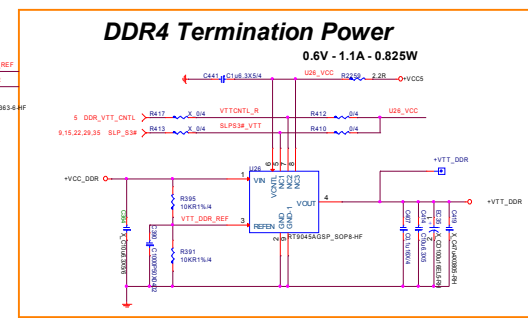


DDR4 I/O power decoupling caps.



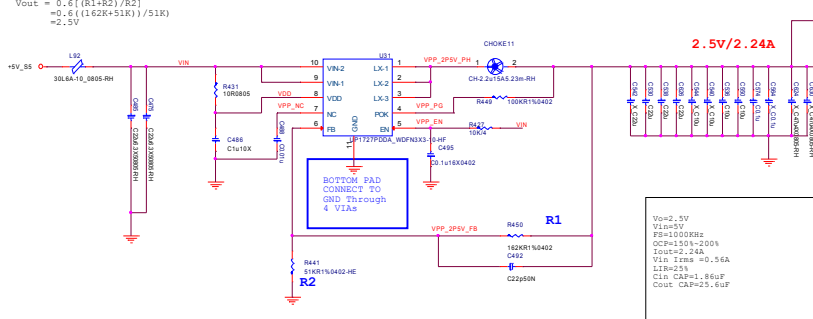
DDR4 Termination Power

0.6V - 1.1A - 0.825W

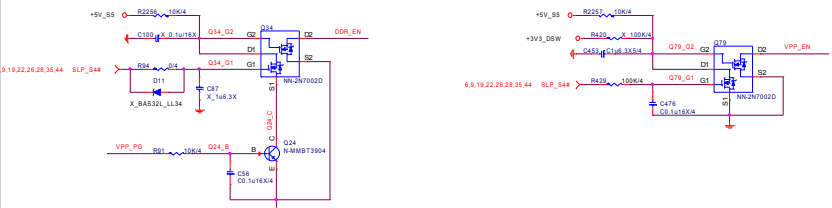
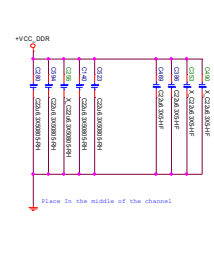
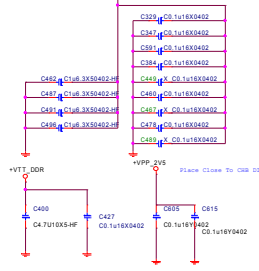
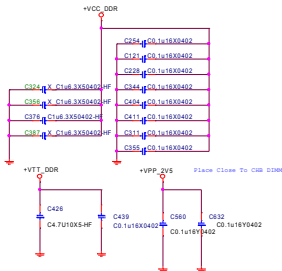
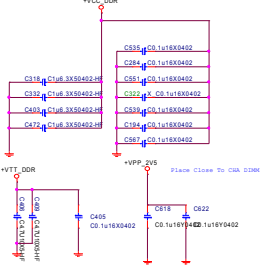


VPP_2.5V

$$V_{out} = 0.6 \left(\frac{R1+R2}{R2} \right) \\ = 0.6 \left(\frac{162K+51K}{51K} \right) \\ = 2.5V$$

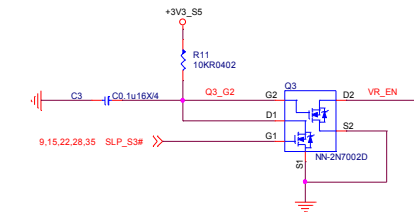


VDD=2.5V
VDDQ=2.5V
FDD=300kHz
OCP=150%~200%
Iout=2.24A
VDDQ Itrms=0.56A
LTR=251
CIn CAP=1.86uF
Cout CAP=25.6uF

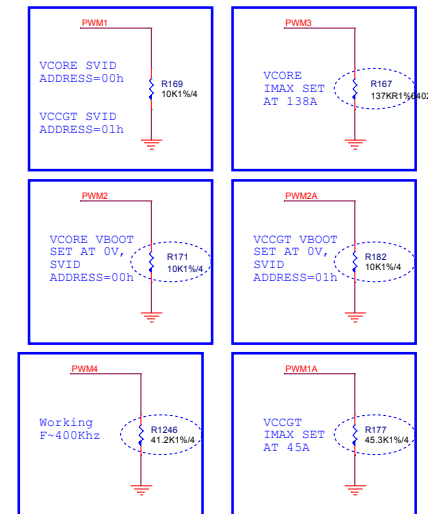
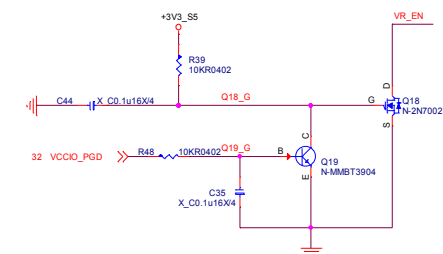


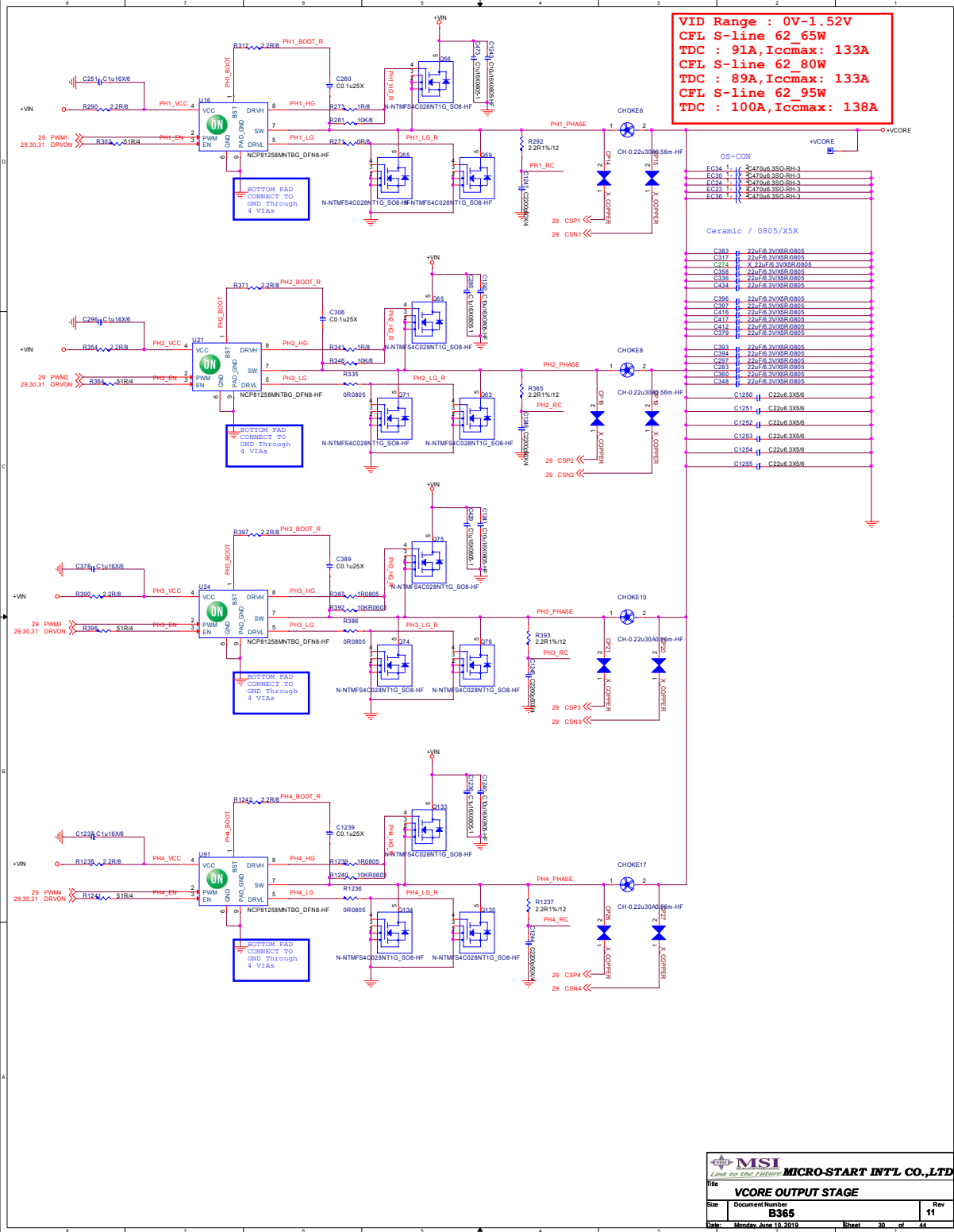
Power Sequence

O/P Choke:
0.3uH/0.6m

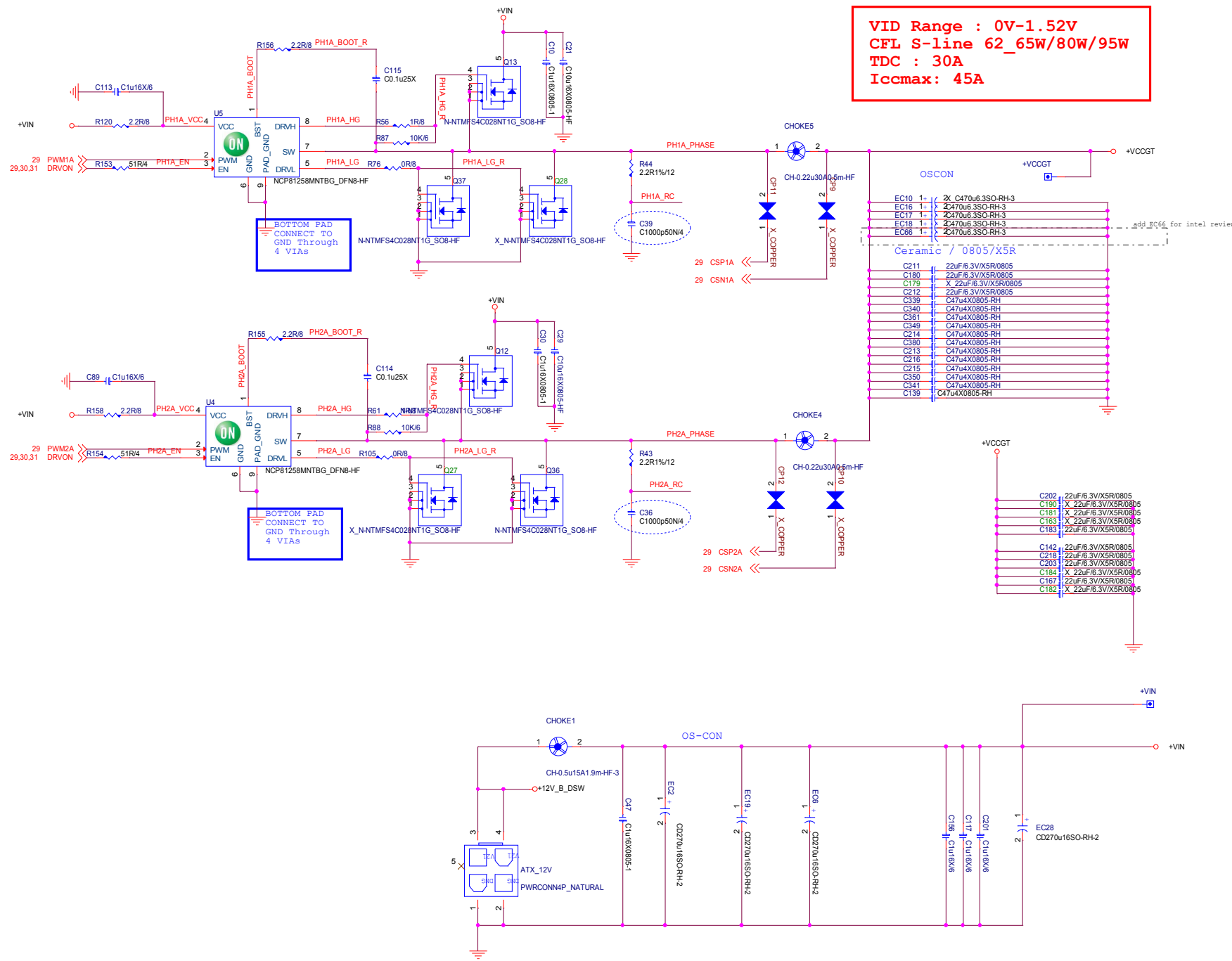


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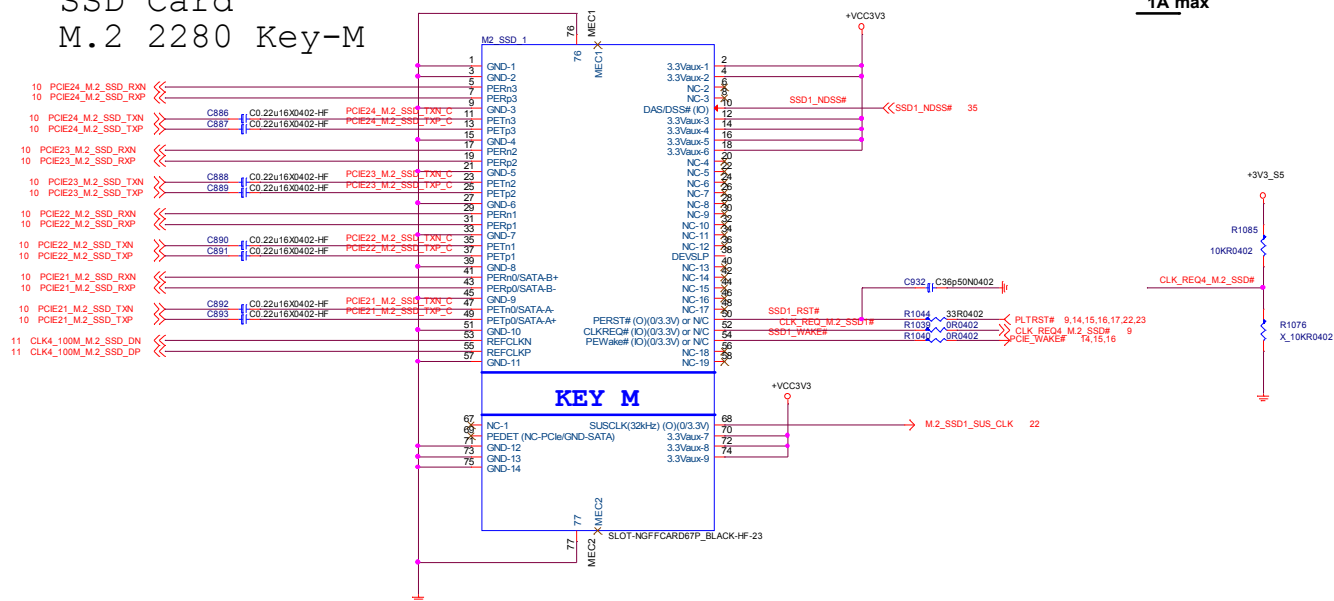




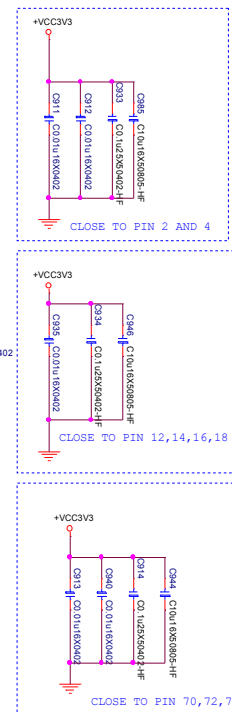
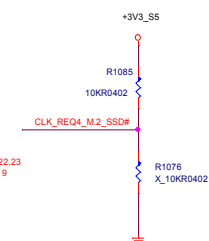
VID Range : 0V-1.52V
CFL S-line 62_65W/80W/95W
TDC : 30A
Iccmax: 45A



SSD	Card	
M.2	2280	Key-M



1A max

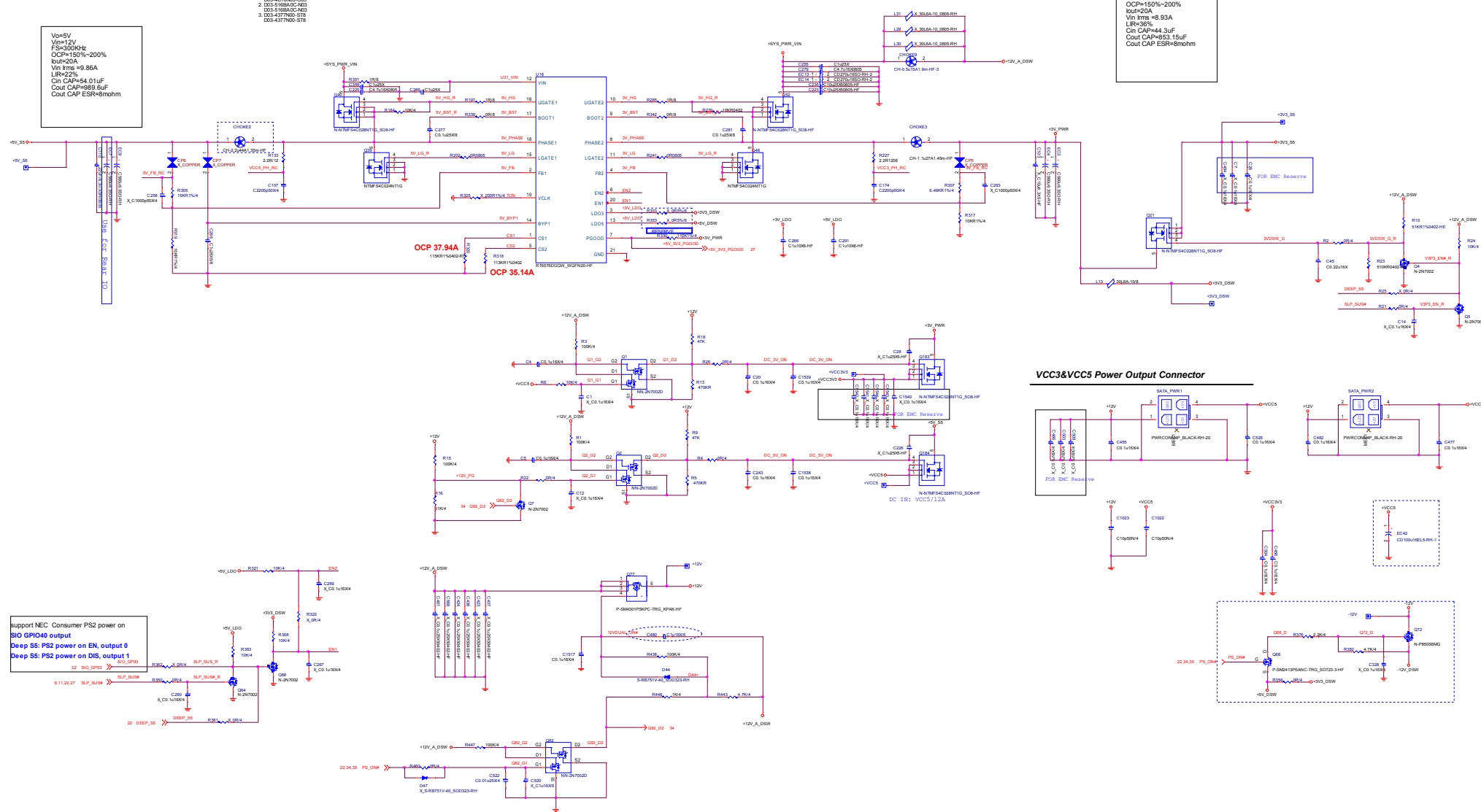


```

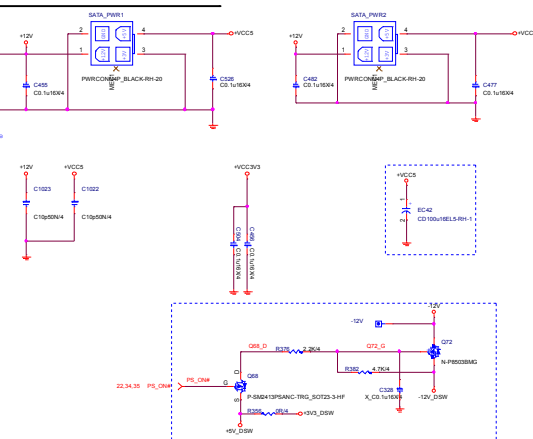
EC Consumer PS2 power on
040 output
: PS2 power on EN, output 0
: PS2 power on DIS, output 1

```

Vo=3.3V
Vin=12V
FS=300KHz
OCP=150%~200%
Iout=20A
Vin Irms =8.93A
LIR=36%
Cin CAP=44.3uF
Cout CAP=853.15uF
Cout CAP ESR=8mohm

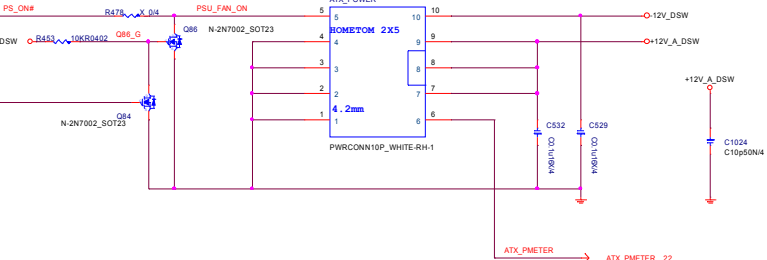


FOR EMC Reserve

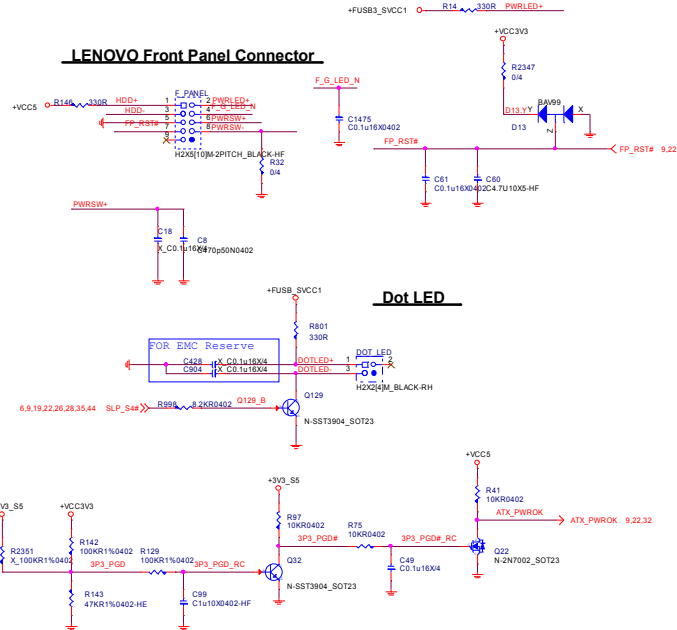


8 Pin ATX Power Connector

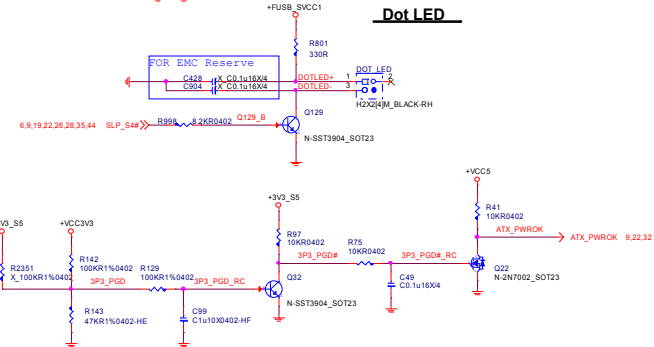
Power Supply in mounted



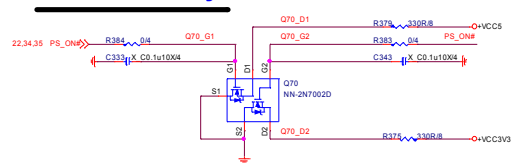
LENOVO Front Panel Connector



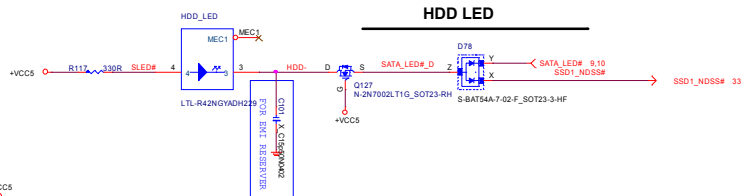
Dot LED



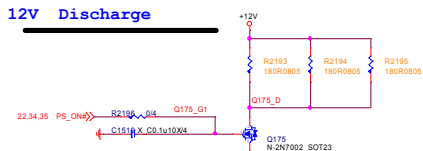
VCC3/VCC5 Discharge



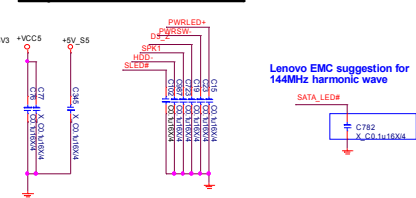
HDD LED



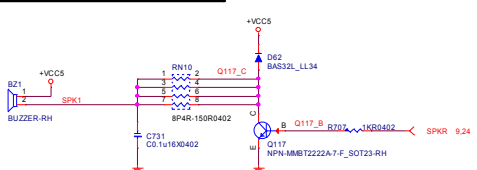
12V Discharge



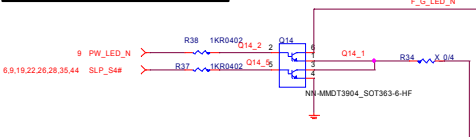
Cap For EMI




Buzzer Circuit



Power LED

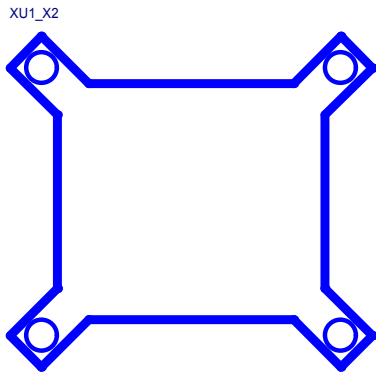
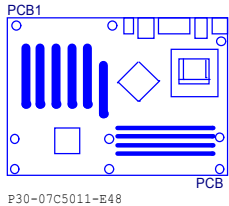


HD (IDE Hard Disk Active LED)	Pin 1:LED anode(+) Pin 8:LED cathode(-)
(Power LED)	Pin 3:LED cathode(-) (green) Pin 2:LED cathode(-) (yellow)
Power Switch	Open:Normal Operation Close:Power on /Off

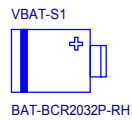
 **MSI**
Link to the Future **MICRO-START INTL CO., LTD**

Title		ATX/F_Panel/EMI/LED	
Size	Document Number	Rev	
	B365	11	
Date:	Monday, June 03, 2019	Sheet	35 of 44

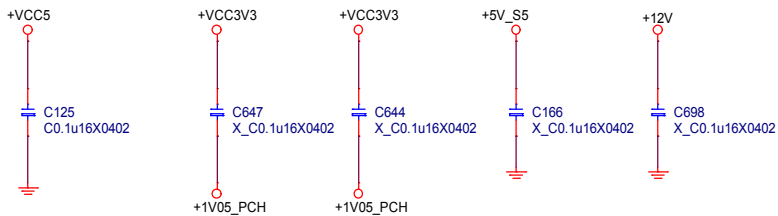
Manual Parts



X_CPU Backplate

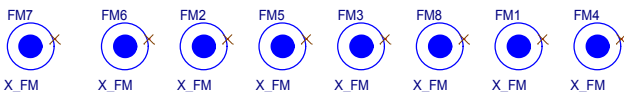


For EMI For Moat CAP



Optics Orientation Holes

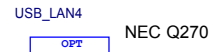
Optical Fiducial Marks-120



with surge single LED +USB3.0 X2 connector: N58-30F0151-F02



without surge +USB3.0 X2 connector: N58-32F0531-S42



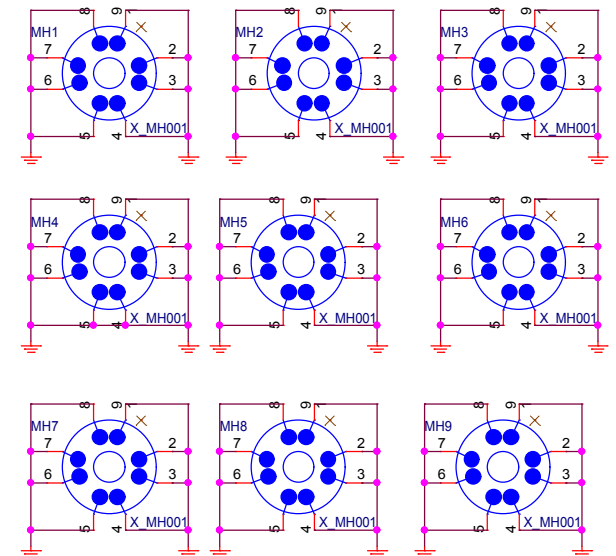
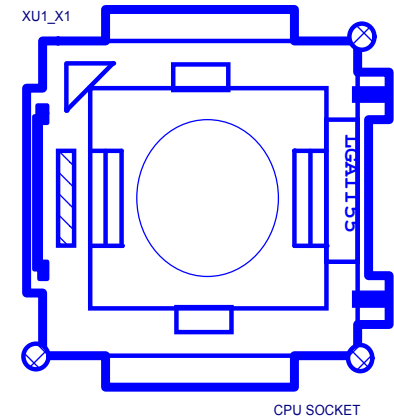
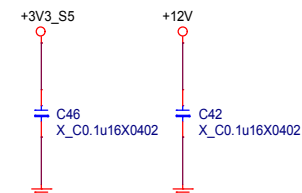
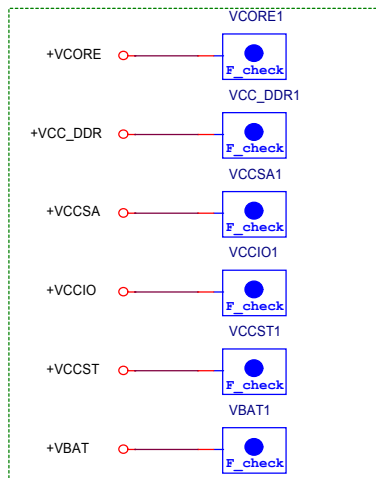
without surge +USB3.0 X2 connector: N58-32F0221-F02

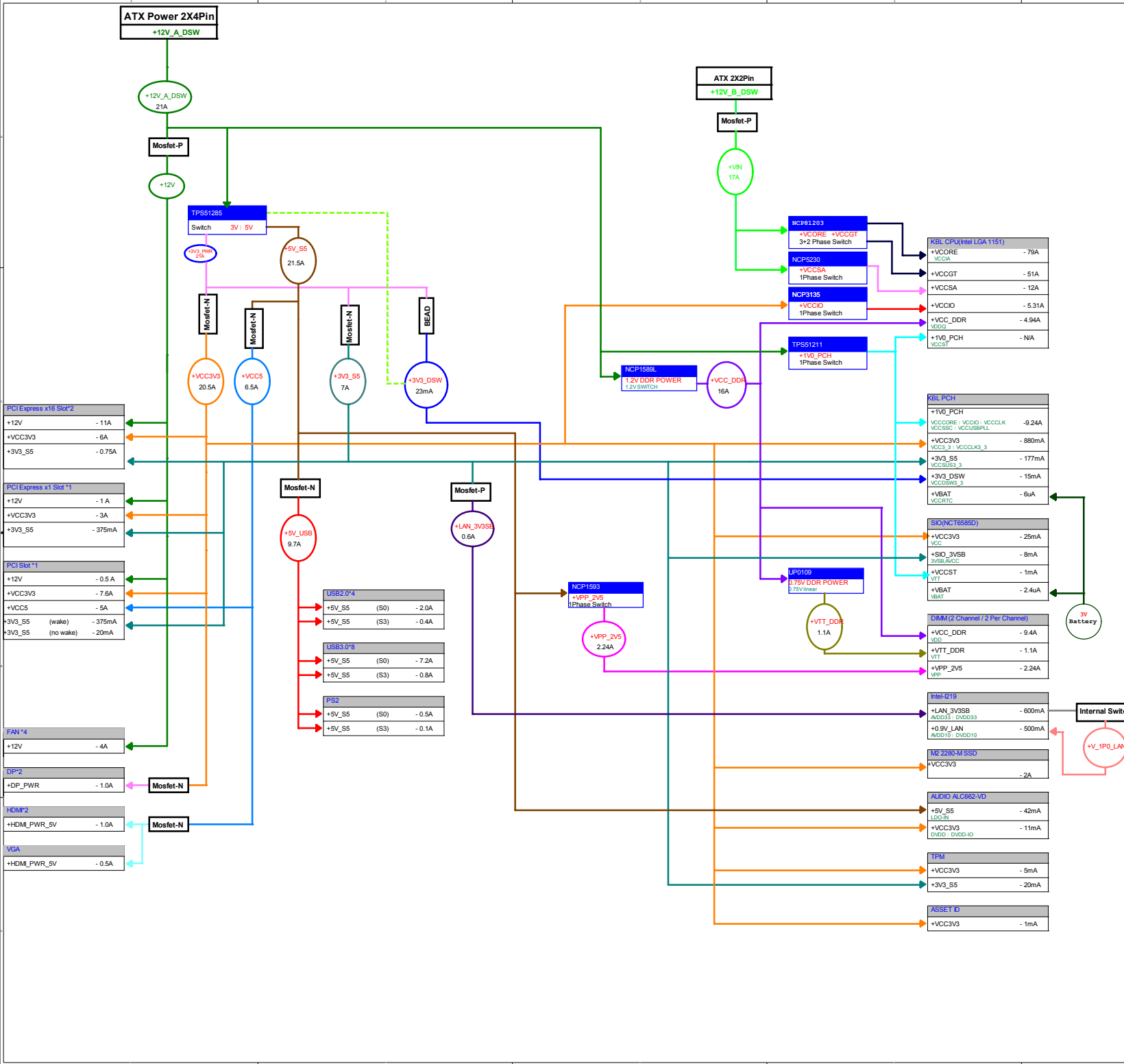


without surge +USB2.0 X2 connector: N58-27F0021-F02

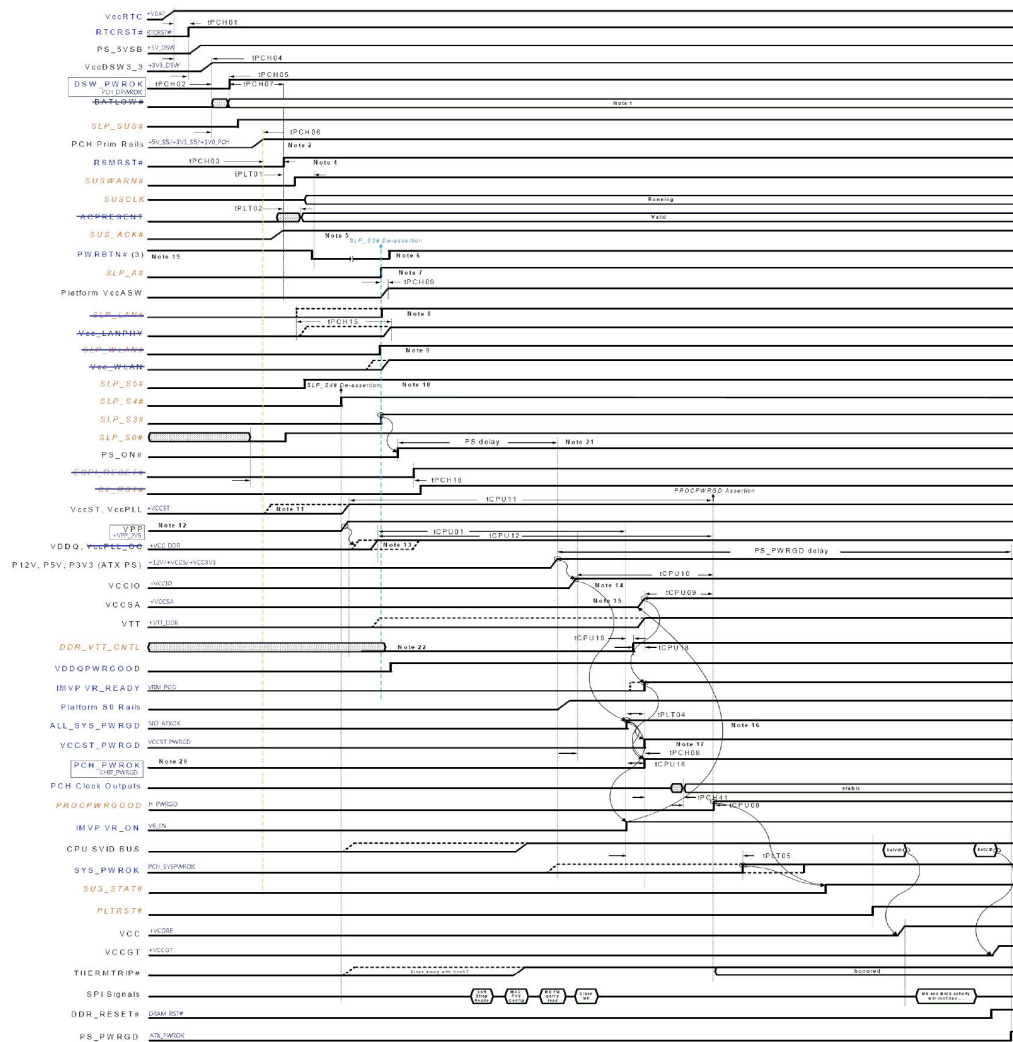


with surge single LED +USB2.0 X2 connector: N58-25F0291-F02

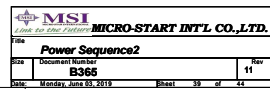


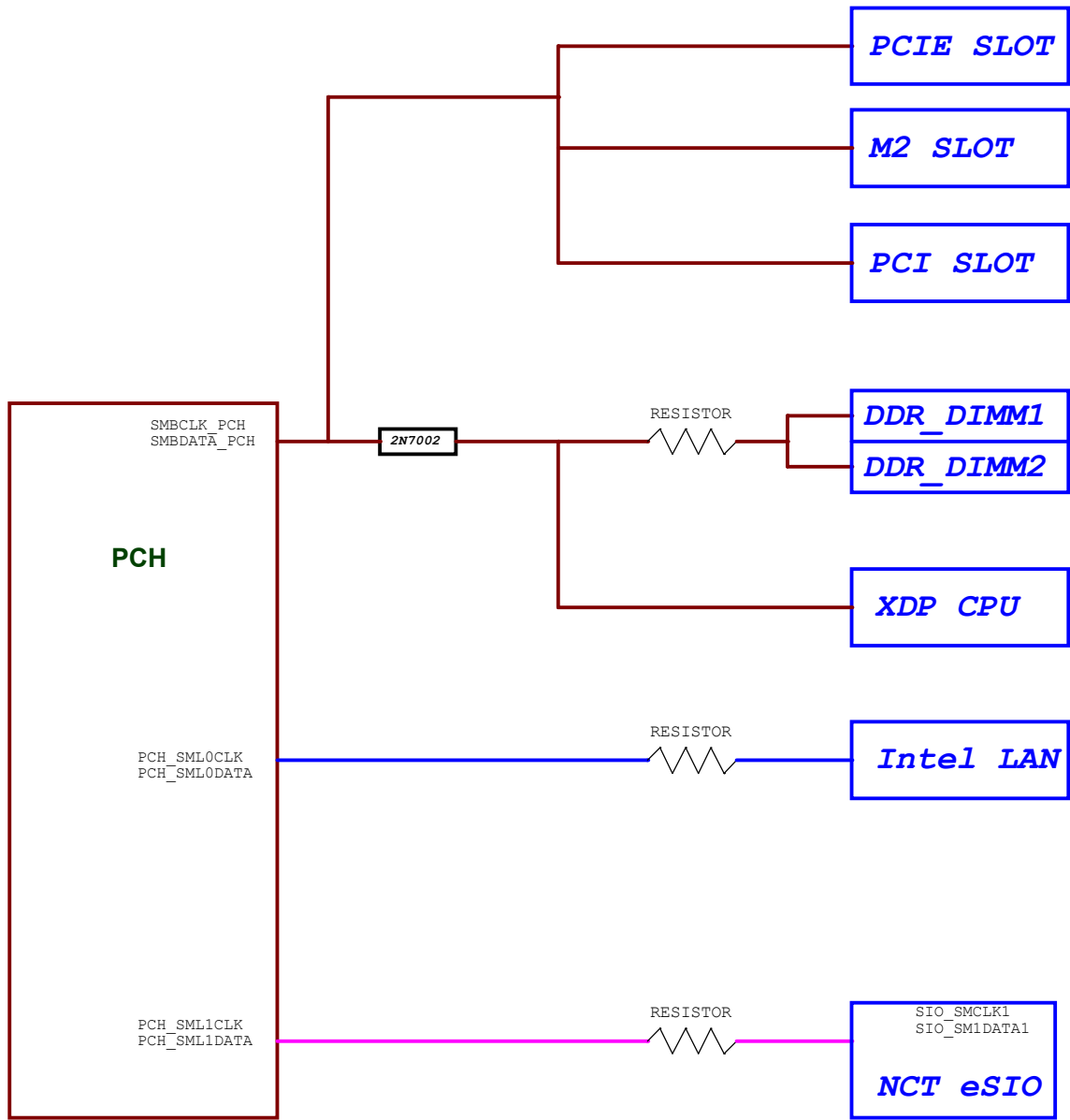


SKL-S Timing Diagram for G3 to S0 [Deep Sx Platform]

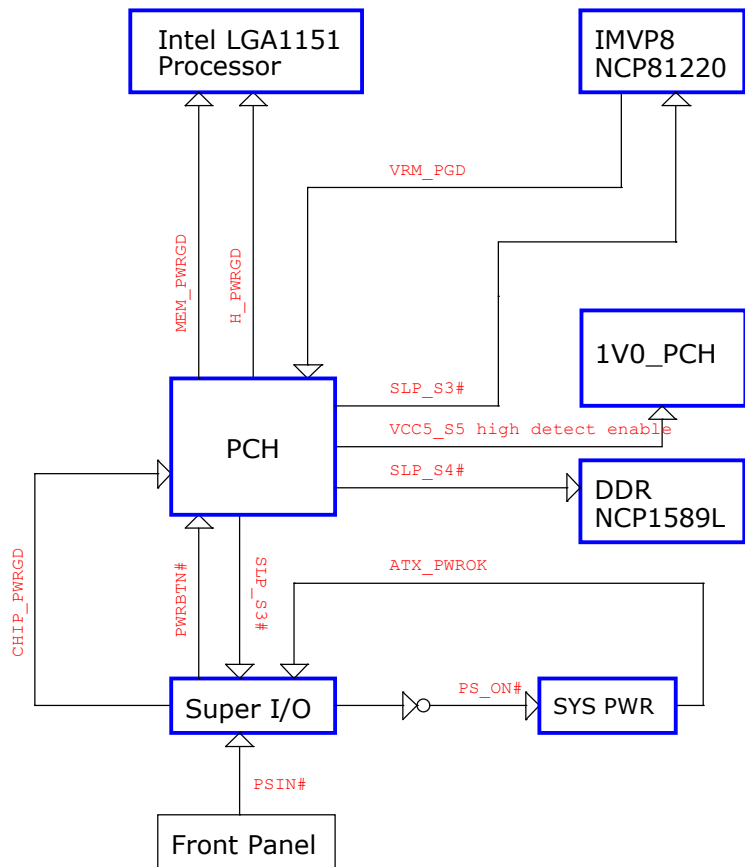


with Deep Sx support			G3	DEEP S5	S0
source	destination				
board	PCH	VBAT			
board	PCH	RTCST#			
PSU	board	+5VSB_DSW			
board	PCH	+3VSB_DSW			
board	PCH	PCH_DPWROK			
PCH	SIO	PCH_SUSWARN#			
SIO	PCH	PCH_SUSACK#			
PCH	SIO	SLE_SUS#			
board	board	+5V_S5			
board	PCH	+3V3_S5			
board	PCH	+1V0_PCH			
SIO	PCH	RSMRST#			

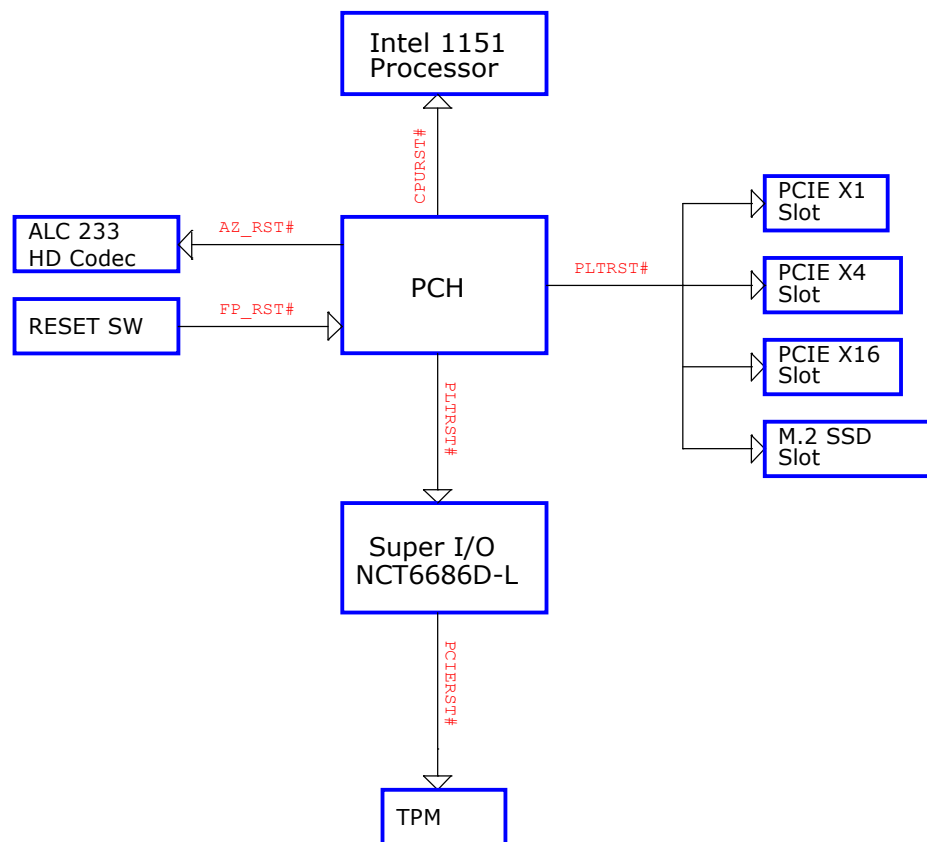




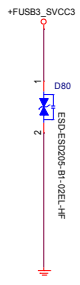
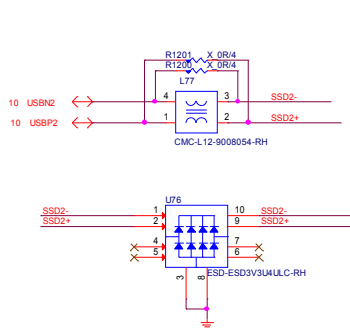
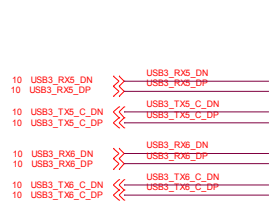
PWROK MAP



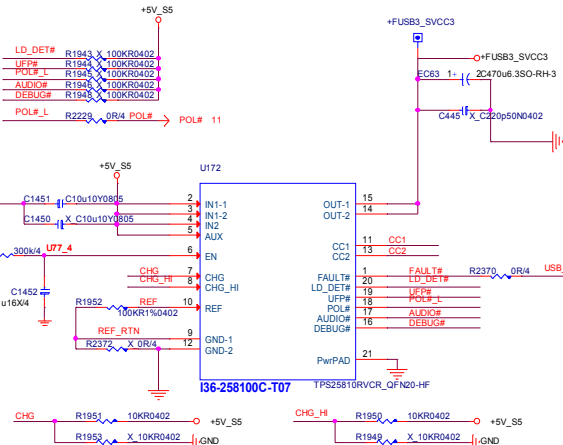
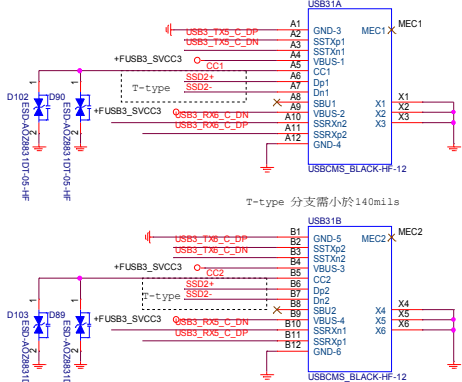
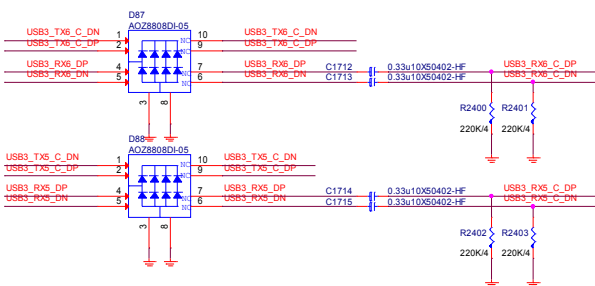
RESET MAP



GPIO				GPIO				GPIO				GPIO			
Signal Name	Power Well	IN/OUT	Usage	Signal Name	Power Well	IN/OUT	Usage	Signal Name	Power Well	IN/OUT	Usage	Signal Name	Power Well	IN/OUT	Usage
GPIO A0	GPIO A0, RCIN, N_ESPI_ALERT1_N	SB3V	Native HBRST	GPIO D0	GPIO D0, SPI1_CS_N	SB3V	Native N.C	GPIO D0	GPIO D0, FAN_TACH_0	SB3V	Native N.C	GPIO D0	GPIO D0, FAN_TACH_0	SB3V	Native N.C
GPIO A1	GPIO A1, LADD_ESPI_L00	SB3V	Native LPC_A00	GPIO D1	GPIO D1, SPI1_CLK	SB3V	OUT PW_LED_N	GPIO D1	GPIO D1, FAN_TACH_1	SB3V	IN CHASSIS_D0	GPIO D1	GPIO D1, FAN_TACH_1	SB3V	IN CHASSIS_D0
GPIO A2	GPIO A2, LADD_ESPI_L01	SB3V	Native LPC_A01	GPIO D2	GPIO D2, SPI1_MISO	SB3V	IN PD_PCH_GPIO_D_2	GPIO D2	GPIO D2, FAN_TACH_2	SB3V	IN T_HOCHOT_PCH_N	GPIO D2	GPIO D2, FAN_TACH_2	SB3V	IN T_HOCHOT_PCH_N
GPIO A3	GPIO A3, LADD_ESPI_L02	SB3V	Native LPC_A02	GPIO D3	GPIO D3, SPI1_MOSI	SB3V	IN PD_PCH_GPIO_D_3	GPIO D3	GPIO D3, FAN_TACH_3	SB3V	Native PCH_BMC_FORCE_INT_N	GPIO D3	GPIO D3, FAN_TACH_3	SB3V	Native PCH_BMC_FORCE_INT_N
GPIO A4	GPIO A4, LADD_ESPI_L03	SB3V	Native LPC_A03	GPIO D4	GPIO D4, I2H_I2C2_SDA	SB3V	OUT BUS_LED_N	GPIO D4	GPIO D4, FAN_TACH_4	SB3V	Native N.C	GPIO D4	GPIO D4, FAN_TACH_4	SB3V	Native N.C
GPIO A5	GPIO A5, FRAME_I2_ESPI_CS_N	SB3V	Native LPC_FRAME	GPIO D5	GPIO D5, I2C2_SDA	SB3V	Native N.C	GPIO D5	GPIO D5, FAN_TACH_5	SB3V	Native N.C	GPIO D5	GPIO D5, FAN_TACH_5	SB3V	Native N.C
GPIO A6	GPIO A6, SERIRQ	SB3V	Native LPC_SERIRQ	GPIO D6	GPIO D6, SPI0_TID	SB3V	Native N.C	GPIO D6	GPIO D6, FAN_TACH_6	SB3V	Native N.C	GPIO D6	GPIO D6, FAN_TACH_6	SB3V	Native N.C
GPIO A7	GPIO A7, FRIDA_N_ESPI_ALERT0_N	SB3V	Native LPC_DRQ00	GPIO D7	GPIO D7, SPI0_R0D	SB3V	Native N.C	GPIO D7	GPIO D7, FAN_TACH_7	SB3V	Native N.C	GPIO D7	GPIO D7, FAN_TACH_7	SB3V	Native N.C
GPIO A8	GPIO A8, CLKIN_N	SB3V	Native CLKIN_N	GPIO D8	GPIO D8, SPI0_CLK	SB3V	Native N.C	GPIO D8	GPIO D8, FAN_PWN_0	SB3V	Native N.C	GPIO D8	GPIO D8, FAN_PWN_0	SB3V	Native N.C
GPIO A9	GPIO A9, CLKOUT_EP00_ESPI_CLK	SB3V	Native LEO_CHIP_CLK	GPIO D9	GPIO D9, I2H_SPL_CS_N	SB3V	Native N.C	GPIO D9	GPIO D9, FAN_PWN_1	SB3V	Native N.C	GPIO D9	GPIO D9, FAN_PWN_1	SB3V	Native N.C
GPIO A10	GPIO A10, CLKOUT_LPC1	SB3V	Native PCH_CLK_24M	GPIO D10	GPIO D10, I2H_SPL_CLK	SB3V	Native N.C	GPIO D10	GPIO D10, FAN_PWN_2	SB3V	Native N.C	GPIO D10	GPIO D10, FAN_PWN_2	SB3V	Native N.C
GPIO A11	GPIO A11, FINE_N	SB3V	Native SIO_RIP#	GPIO D11	GPIO D11, I2H_SPL_MOSI	SB3V	IN FUSB_01	GPIO D11	GPIO D11, FAN_PAWN_3	SB3V	IN BMC_THROTTLE_N	GPIO D11	GPIO D11, FAN_PAWN_3	SB3V	IN BMC_THROTTLE_N
GPIO A12	GPIO A12, HIBUSBY_N	SB3V	Native HIBUSBY#	GPIO D12	GPIO D12, I2H_SPL_MOSI	SB3V	IN FUSB_02	GPIO D12	GPIO D12, I2SOUT	SB3V	IN GPP_00	GPIO D12	GPIO D12, I2SOUT	SB3V	IN GPP_00
GPIO A13	GPIO A13, SUSIRQ_N, SUSPHRACK	SB3V	Native PCH_SUSWRN#	GPIO D13	GPIO D13, I2H_UART0_RXD	SB3V	IN FUSB_03	GPIO D13	GPIO D13, I2SCLK	SB3V	IN GPP_01	GPIO D13	GPIO D13, I2SCLK	SB3V	IN GPP_01
GPIO A14	GPIO A14, SUS_STAT_N, ESPI_RST_N	SB3V	Native SUS_STAT#	GPIO D14	GPIO D14, I2H_UART0_TXD	SB3V	IN P2C_PCH_HEADER_N	GPIO D14	GPIO D14, I2SDIN	SB3V	IN GPP_02	GPIO D14	GPIO D14, I2SDIN	SB3V	IN GPP_02
GPIO A15	GPIO A15, SUSACK_N	SB3V	Native PCH_SUSACK#	GPIO D15	GPIO D15, I2H_UART0_RTS_N	SB3V	IN LPT_DET#	GPIO D15	GPIO D15, I2SRESET_N	SB3V	IN GPP_03	GPIO D15	GPIO D15, I2SRESET_N	SB3V	IN GPP_03
GPIO A16	GPIO A16, CLKOUT_A6	SB3V	Native N.C	GPIO D16	GPIO D16, I2H_UART1_CTS_N	SB3V	Native N.C	GPIO D16	GPIO D16, I2SCLK	SB3V	IN GPP_04	GPIO D16	GPIO D16, I2SCLK	SB3V	IN GPP_04
GPIO A17	GPIO A17, I2H_GPI	SB3V	OUT BT_DISABLE_N	GPIO D17	GPIO D17, DMIC_CLK1	SB3V	Native COM_WAKEN	GPIO D17	GPIO D17, ADC_COMPLETE	SB3V	IN GPP_05	GPIO D17	GPIO D17, ADC_COMPLETE	SB3V	IN GPP_05
GPIO A18	GPIO A18, I2H_GPO	SB3V	IN OEN#	GPIO D18	GPIO D18, DMIC_DATA1	SB3V	IN PCH_GPIO_D18	GPIO D18	GPIO D18, NM_I	SB3V	Native FM_NMI_EVENT_N	GPIO D18	GPIO D18, NM_I	SB3V	Native FM_NMI_EVENT_N
GPIO A19	GPIO A19, I2H_GPI	SB3V	Native N.C	GPIO D19	GPIO D19, DMIC_CLK2	SB3V	Native N.C	GPIO D19	GPIO D19, SMI_N	SB3V	IN SIO_SCL_N	GPIO D19	GPIO D19, SMI_N	SB3V	IN SIO_SCL_N
GPIO A20	GPIO A20, I2H_GPO	SB3V	OUT SEL#	GPIO D20	GPIO D20, DMIC_DATA0	SB3V	Native N.C	GPIO D20	GPIO D20, I2SOUT	SB3V	Native BMC_READY	GPIO D20	GPIO D20, I2SOUT	SB3V	Native BMC_READY
GPIO A21	GPIO A21, I2H_GPO	SB3V	IN WLAN_DETECT_N	GPIO D21	GPIO D21, SPI1_I2C	SB3V	Native N.C	GPIO D21	GPIO D21, I2SOUT	SB3V	IN PCH_GPIO20	GPIO D21	GPIO D21, I2SOUT	SB3V	IN PCH_GPIO20
GPIO A22	GPIO A22, I2H_GPI	SB3V	IN I2C0_GPIO	GPIO D22	GPIO D22, SPI1_I2C	SB3V	Native N.C	GPIO D22	GPIO D22, I2SOUT	SB3V	Native PCH_CAM_DET_R_N	GPIO D22	GPIO D22, I2SOUT	SB3V	Native PCH_CAM_DET_R_N
GPIO A23	GPIO A23, I2H_GPO	SB3V	IN LEO_CHIP_GPIO	GPIO D23	GPIO D23, I2H_I2C2_SCL	SB3V	Native N.C	GPIO D23	GPIO D23, I2SOUT	SB3V	OUT VGA_UR0B0	GPIO D23	GPIO D23, I2SOUT	SB3V	OUT VGA_UR0B0
GPIO B0	GPIO B0, CPU_GPIO	SB3V	Native N.C	GPIO E0	GPIO E0, SATA0P0_CIE, SATA0P1	SB3V	Native N.C	GPIO E0	GPIO E0, I2C0_SCL	SB3V	Native N.C	GPIO E0	GPIO E0, I2C0_SCL	SB3V	Native N.C
GPIO B1	GPIO B1	SB3V	Native N.C	GPIO E1	GPIO E1, SATA0P0_CIE, SATA0P1	SB3V	Native N.C	GPIO E1	GPIO E1, I2C0_SCL	SB3V	Native N.C	GPIO E1	GPIO E1, I2C0_SCL	SB3V	Native N.C
GPIO B2	GPIO B2, VREALERT_N	SB3V	Native PCH_VREALERT#	GPIO E2	GPIO E2, SATA0P0_CIE, SATA0P1	SB3V	Native N.C	GPIO E2	GPIO E2, I2C0_SCL	SB3V	Native N.C	GPIO E2	GPIO E2, I2C0_SCL	SB3V	Native N.C
GPIO B3	GPIO B3, CPU_GPIO	SB3V	Native N.C	GPIO E3	GPIO E3, CPU_GPIO	SB3V	Native BMC_PCH_SCL_N	GPIO E3	GPIO E3, I2C0_SCL	SB3V	Native N.C	GPIO E3	GPIO E3, I2C0_SCL	SB3V	Native N.C
GPIO B4	GPIO B4, CPU_GPIO	SB3V	Native N.C	GPIO E4	GPIO E4, DEVSUP	SB3V	Native BMC_FORCE_SMI_N	GPIO E4	GPIO E4, I2C0_SCL	SB3V	Native N.C	GPIO E4	GPIO E4, I2C0_SCL	SB3V	Native N.C
GPIO B5	GPIO B5, SRCCLOCK0_N	SB3V	IN PCH_VREALERT#	GPIO E5	GPIO E5, DEVSUP	SB3V	Native N.C	GPIO E5	GPIO E5, I2C0_SCL	SB3V	Native N.C	GPIO E5	GPIO E5, I2C0_SCL	SB3V	Native N.C
GPIO B6	GPIO B6, SRCCLOCK0_N	SB3V	Native PCH_VREALERT#	GPIO E6	GPIO E6, DEVSUP	SB3V	Native N.C	GPIO E6	GPIO E6, I2C0_SCL	SB3V	Native N.C	GPIO E6	GPIO E6, I2C0_SCL	SB3V	Native N.C
GPIO B7	GPIO B7, SRCCLOCK0_N	SB3V	IN PCH_VREALERT#	GPIO E7	GPIO E7, CPU_GPIO	SB3V	Native N.C	GPIO E7	GPIO E7, I2C0_SCL	SB3V	Native N.C	GPIO E7	GPIO E7, I2C0_SCL	SB3V	Native N.C
GPIO B8	GPIO B8, SRCCLOCK0_N	SB3V	IN CLKIN_N, I2C0_SCL	GPIO E8	GPIO E8, DEVSUP	SB3V	Native N.C	GPIO E8	GPIO E8, I2C0_SCL	SB3V	Native N.C	GPIO E8	GPIO E8, I2C0_SCL	SB3V	Native N.C
GPIO B9	GPIO B9, SRCCLOCK0_N	SB3V	Native N.C	GPIO E9	GPIO E9, I2C0_SCL	SB3V	Native N.C	GPIO E9	GPIO E9, I2C0_SCL	SB3V	Native N.C	GPIO E9	GPIO E9, I2C0_SCL	SB3V	Native N.C
GPIO B10	GPIO B10, SRCCLOCK0_N	SB3V	Native N.C	GPIO E10	GPIO E10, I2C0_SCL	SB3V	Native N.C	GPIO E10	GPIO E10, I2C0_SCL	SB3V	Native N.C	GPIO E10	GPIO E10, I2C0_SCL	SB3V	Native N.C
GPIO B11	GPIO B11	SB3V	Native N.C	GPIO E11	GPIO E11, I2C0_SCL	SB3V	Native N.C	GPIO E11	GPIO E11, I2C0_SCL	SB3V	Native N.C	GPIO E11	GPIO E11, I2C0_SCL	SB3V	Native N.C
GPIO B12	GPIO B12, SLP_S0_N	SB3V	Native SLP_S0#	GPIO E12	GPIO E12, I2C0_SCL	SB3V	Native N.C	GPIO E12	GPIO E12, I2C0_SCL	SB3V	Native N.C	GPIO E12	GPIO E12, I2C0_SCL	SB3V	Native N.C
GPIO B13	GPIO B13, PLTRST#	SB3V	Native PLTRST#	GPIO E13	GPIO E13, I2C0_SCL	SB3V	Native N.C	GPIO E13	GPIO E13, I2C0_SCL	SB3V	Native N.C	GPIO E13	GPIO E13, I2C0_SCL	SB3V	Native N.C
GPIO B14	GPIO B14, SPWR	SB3V	Native SPWR	GPIO E14	GPIO E14, I2C0_SCL	SB3V	Native N.C	GPIO E14	GPIO E14, I2C0_SCL	SB3V	Native N.C	GPIO E14	GPIO E14, I2C0_SCL	SB3V	Native N.C
GPIO B15	GPIO B15, SPI0_CS_N	SB3V	Native N.C	GPIO E15	GPIO E15, I2C0_SCL	SB3V	Native N.C	GPIO E15	GPIO E15, I2C0_SCL	SB3V	Native N.C	GPIO E15	GPIO E15, I2C0_SCL	SB3V	Native N.C
GPIO B16	GPIO B16, SPI0_CLK	SB3V	Native N.C	GPIO E16	GPIO E16, I2C0_SCL	SB3V	Native N.C	GPIO E16	GPIO E16, I2C0_SCL	SB3V	Native N.C	GPIO E16	GPIO E16, I2C0_SCL	SB3V	Native N.C
GPIO B17	GPIO B17, SPI0_MISO	SB3V	Native N.C	GPIO E17	GPIO E17, I2C0_SCL	SB3V	Native N.C	GPIO E17	GPIO E17, I2C0_SCL	SB3V	Native N.C	GPIO E17	GPIO E17, I2C0_SCL	SB3V	Native N.C
GPIO B18	GPIO B18, SPI0_MOSI	SB3V	Native REBOOT_STRAP	GPIO E18	GPIO E18, I2C0_SCL	SB3V	Native N.C	GPIO E18	GPIO E18, I2C0_SCL	SB3V	Native N.C	GPIO E18	GPIO E18, I2C0_SCL	SB3V	Native N.C
GPIO B19	GPIO B19, SPI0_CS_N	SB3V	Native N.C	GPIO E19	GPIO E19, I2C0_SCL	SB3V	Native N.C	GPIO E19	GPIO E19, I2C0_SCL	SB3V	Native N.C	GPIO E19	GPIO E19, I2C0_SCL	SB3V	Native N.C
GPIO B20	GPIO B20, SPI0_CLK	SB3V	IN SMI#	GPIO E20	GPIO E20, I2C0_SCL	SB3V	Native N.C	GPIO E20	GPIO E20, I2C0_SCL	SB3V	Native N.C	GPIO E20	GPIO E20, I2C0_SCL	SB3V	Native N.C
GPIO B21	GPIO B21, SPI0_MISO	SB3V	Native N.C	GPIO E21	GPIO E21, I2C0_SCL	SB3V	Native N.C	GPIO E21	GPIO E21, I2C0_SCL	SB3V	Native N.C	GPIO E21	GPIO E21, I2C0_SCL	SB3V	Native N.C
GPIO B22	GPIO B22, SPI0_MOSI	SB3V	IN I2C0_SCL	GPIO E22	GPIO E22, I2C0_SCL	SB3V	Native N.C	GPIO E22	GPIO E22, I2C0_SCL	SB3V	Native N.C	GPIO E22	GPIO E22, I2C0_SCL	SB3V	Native N.C
GPIO B23	GPIO B23, SMI_ALERT_N, PCH_HOT_N	SB3V	IN SMI_ALERT_N	GPIO E23	GPIO E23, I2C0_SCL	SB3V	Native N.C	GPIO E23	GPIO E23, I2C0_SCL	SB3V	Native N.C	GPIO E23	GPIO E23, I2C0_SCL	SB3V	Native N.C
GPIO C0	GPIO C0, SMI0CLK	SB3V	Native SMI0CLK#	GPIO E24	GPIO E24, I2C0_SCL	SB3V	Native N.C	GPIO E24	GPIO E24, I2C0_SCL	SB3V	Native N.C	GPIO E24	GPIO E24, I2C0_SCL	SB3V	Native N.C
GPIO C1	GPIO C1, SMI0DATA	SB3V	Native SMI0DATA#	GPIO E25	GPIO E25, I2C0_SCL	SB3V	Native N.C	GPIO E25	GPIO E25, I2C0_SCL	SB3V	Native N.C	GPIO E25	GPIO E25, I2C0_SCL	SB3V	Native N.C
GPIO C2	GPIO C2, SMI0ALERT_N	SB3V	Native I2S_STRAP	GPIO E26	GPIO E26, I2C0_SCL	SB3V	Native N.C	GPIO E26	GPIO E26, I2C0_SCL	SB3V	Native N.C	GPIO E26	GPIO E26, I2C0_SCL	SB3V	Native N.C
GPIO C3	GPIO C3, SMI0DATA	SB3V	Native SMI0_DATA	GPIO E27	GPIO E27, I2C0_SCL	SB3V	Native N.C	GPIO E27	GPIO E27, I2C0_SCL	SB3V	Native N.C	GPIO E27	GPIO E27, I2C0_SCL	SB3V	Native N.C
GPIO C4	GPIO C4, SMI0ALERT_N	SB3V	Native SMI0_STRAP	GPIO E28	GPIO E28, I2C0_SCL	SB3V	Native N.C	GPIO E28	GPIO E28, I2C0_SCL	SB3V	Native N.C	GPIO E28	GPIO E28, I2C0_SCL	SB3V	Native N.C
GPIO C5	GPIO C5, SMI0CLK	SB3V	Native SMI0_CLK	GPIO E29	GPIO E29, I2C0_SCL	SB3V	Native N.C	GPIO E29	GPIO E29, I2C0_SCL	SB3V	Native N.C	GPIO E29	GPIO E29, I2C0_SCL	SB3V	Native N.C
GPIO C6	GPIO C6, SMI0DATA	SB3V	Native SMI0_DATA	GPIO E30	GPIO E30, I2C0_SCL	SB3V	Native N.C	GPIO E30	GPIO E30, I2C0_SCL	SB3V	Native N.C	GPIO E30	GPIO E30, I2C0_SCL	SB3V	Native N.C
GPIO C7	GPIO C7, SMI0ALERT_N	SB3V	Native SMI0_STRAP	GPIO E31	GPIO E31, I2C0_SCL	SB3V	Native N.C	GPIO E31	GPIO E31, I2C0_SCL	SB3V	Native N.C	GPIO E31	GPIO E31, I2C0_SCL	SB3V	Native N.C
GPIO C8	GPIO C8, SMI0CLK	SB3V	Native SMI0_CLK	GPIO E32	GPIO E32, I2C0_SCL	SB3V	Native N.C	GPIO E32	GPIO E32, I2C0_SCL	SB3V	Native N.C	GPIO E32	GPIO E32, I2C0_SCL	SB3V	Native N.C
GPIO C9	GPIO C9, SMI0DATA	SB3V	Native SMI0_DATA	GPIO E33	GPIO E33, I2C0_SCL	SB3V	Native N.C	GPIO E33	GPIO E33, I2C0_SCL	SB3V	Native N.C	GPIO E33	GPIO E33, I2C0_SCL	SB3V	Native N.C
GPIO C10	GPIO C10, SMI0ALERT_N	SB3V	Native SMI0_STRAP	GPIO E34	GPIO E34, I2C0_SCL	SB3V	Native N.C	GPIO E34	GPIO E34, I2C0_SCL	SB3V	Native N.C	GPIO E34	GPIO E34, I2C0_SCL	SB3V	Native N.C
GPIO C11	GPIO C11, SMI0CLK	SB3V	Native SMI0_CLK	GPIO E35	GPIO E35, I2C0_SCL	SB3V	Native N.C	GPIO E35	GPIO E35, I2C0_SCL	SB3V	Native N.C	GPIO E35	GPIO E35, I2C0_SCL	SB3V	Native N.C
GPIO C12	GPIO C12, SMI0DATA	SB3V	Native SMI0_DATA	GPIO E36	GPIO E36, I2C0_SCL	SB3V	Native N.C	GPIO E36	GPIO E36, I2C0_SCL	SB3V	Native N.C	GPIO E36	GPIO E36, I2C0_SCL	SB3V	Native N.C
GPIO C13	GPIO C13, SMI0ALERT_N	SB3V	Native SMI0_STRAP	GPIO E37	GPIO E37, I2C0_SCL	SB3V	Native N.C	GPIO E37	GPIO E37, I2C0_SCL	SB3V	Native N.C	GPIO E37	GPIO E37, I2C0_SCL	SB3V	Native N.C
GPIO C14	GPIO C14, SMI0CLK	SB3V	Native SMI0_CLK	GPIO E38	GPIO E38, I2C0_SCL	SB3V	Native N.C	GPIO E38	GPIO E38, I2C0_SCL	SB3V	Native N.C	GPIO E38	GPIO E38, I2C0_SCL	SB3V	Native N.C
GPIO C15	GPIO C15, SMI0DATA	SB3V	Native SMI0_DATA	GPIO E39	GPIO E39, I2C0_SCL	SB3V	Native N.C	GPIO E39	GPIO E39, I2C0_SCL	SB3V	Native N.C	GPIO E39	GPIO E39, I2C0_SCL	SB3V	Native N.C
GPIO C16	GPIO C16, SMI0ALERT_N	SB3V	Native SMI0_STRAP	GPIO E40	GPIO E40, I2C0_SCL	SB3V	Native N.C	GPIO E40	GPIO E40, I2C0_SCL	SB3V	Native N.C	GPIO E40	GPIO E40, I2C0_SCL	SB3V	Native N.C
GPIO C17	GPIO C17, SMI0CLK	SB3V	Native SMI0_CLK	GPIO E41	GPIO E41, I2C0_SCL	SB3V	Native N.C	GPIO E41	GPIO E41, I2C0_SCL	SB3V	Native N.C	GPIO E41	GPIO E41, I2C0_SCL	SB3V	Native N.C
GPIO C18	GPIO C18, SMI0DATA	SB3V	Native SMI0_DATA	GPIO E42	GPIO E42, I2C0_SCL	SB3V	Native N.C	GPIO E42	GPIO E42, I2C0_SCL	SB3V	Native N.C	GPIO E42	GPIO E42, I2C0_SCL	SB3V	Native N.C
GPIO C19	GPIO C19, SMI0ALERT_N	SB3V	Native SMI0_STRAP	GPIO E43	GPIO E43, I2C0_SCL	SB3V	Native N.C	GPIO E43	GPIO E43, I2C0_SCL	SB3V	Native N.C	GPIO E43	GPIO E43, I2C0_SCL	SB3V	Native N.C
GPIO C20	GPIO C20, SMI0CLK	SB3V	Native SMI0_CLK	GPIO E44	GPIO E44, I2C0_SCL	SB3V	Native N.C	GPIO E44	GPIO E44, I2C0_SCL	SB3V	Native N.C	GPIO E44	GPIO E44, I2C0_SCL	SB3V	Native N.C
GPIO C21	GPIO C21, SMI0DATA	SB3V	Native SMI0_DATA	GPIO E45	GPIO E45, I2C0_SCL	SB3V	Native N.C	GPIO E45	GPIO E45, I2C0_SCL	SB3V	Native N.C	GPIO E45	GPIO E45, I2C0_SCL	SB3V	Native N.C
GPIO C22	GPIO C22, SMI0ALERT_N	SB3V	Native SMI0_STRAP	GPIO E46	GPIO E46, I2C0_SCL	SB3V	Native N.C	GPIO E46	GPIO E46, I2C0_SCL	SB3V	Native N.C	GPIO E46	GPIO E46, I2C0_SCL	SB3V	Native N.C
GPIO C23	GPIO C23, SMI0CLK	SB3V	Native SMI0_CLK	GPIO E47	GPIO E47, I2C0_SCL	SB3V	Native N.C	GPIO E47	GPIO E47, I2C0_SCL	SB3V	Native N.C	GPIO E47	GPIO E47, I2C0_SCL	SB3V	Native N.C
GPIO C24	GPIO C24, SMI0DATA	SB3V	Native SMI0_DATA	GPIO E48	GPIO E48, I2C0_SCL	SB3V	Native N.C	GPIO E48	GPIO E48, I2C0_SCL	SB3V	Native N.C	GPIO E48	GPIO E48, I2C0_SCL	SB3V	Native N.C
GPIO															



ESD Protection NEAR CONNECTOR



CHG	CHG_HI	CC
0	0	STD
0	1	STD
1	0	1.5A
1	1	3A

